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DESIGN ANALYSIS TRACKING AND DATA RELAY SATELLITE SIMULATION SYSTEM

(NASA-CR-139032) DESIGN ANALYSIS TRACKING
AND DATA RELAY SATELLITE SIMULATION 159
SYSTEM (Airborne Instruments Lab.) 154 p
CSCI 22B

N74-28351

Unclas
43502

G3/31

NAS 5-21653

January 1974

Contract No. N00017-72-C-4401

PRICES SUBJECT TO CHANGE

Prepared for
THE JOHN HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
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N O T I C E

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ABSTRACT

The National Aeronautic and Space Administration is moving from the preliminary design of the Tracking and Data Relay Satellite into the execution phase. The design concepts developed over the past few years for the TDRS will thus be realized in hardware. Many of the system concepts are new techniques which have not been fully evaluated in a spaceborne satellite application. To reduce the element of uncertainty in employing these system design concepts, this program was initiated with the objective of simulating the TDRS system.

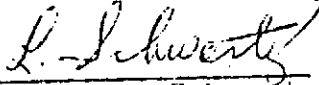
The AIL Division of Cutler-Hammer is under contract from the Applied Physics Laboratory of the John Hopkins University to design and construct the equipment necessary to simulate the S-band Multiple Access link between user spacecraft, the TDRS and a ground control terminal. The core of the S-band Multiple Access concept is the use of an Adaptive Ground Implemented Phased Array (AGIPA), developed by AIL for NASA under Contract NAS-5-21653. The previous adaptive array was a ten channel hard wired system built to determine the feasibility of the concept. The purpose of this program is to expand the adaptive array into a 30 channel system and build the multiplexing and demultiplexing equipment required to demonstrate the ground implemented beam forming feature. The equipment to be provided will enable NASA to demonstrate the performance of a desired user and ten interfering sources attempting to pass data through the multiple access system. Rejection of interference by adaptive nulling and code isolation will be evaluated initially in an AIL test chamber and then on an outdoor test range at APL.

PREFACE

This report is being submitted to the Johns Hopkins University, Applied Physics Laboratory by the AIL Division of Cutler-Hammer Inc. as required under Contract No. 372285. Described herein is the detailed design analysis performed by AIL which is being submitted for APL approval. Work performed from October 1973 to January 1974 is covered in the report.

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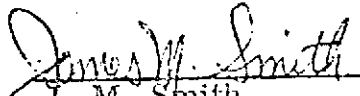

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1.0 INTRODUCTION AND SUMMARY

To verify the performance parameters of the S-band Multiple Access Link for the Tracking and Data Relay Satellite System, a simulation of the TDRS system is being designed and constructed by the AIL Division of Cutler-Hammer. This report presents the design tradeoffs and detailed design of the simulation system.

The simulation system which AIL will deliver to APL basically consists of an expanded Adaptive Ground Implemented Phased Array (AGIPA), * for receiving the multiple access signals, a multiplexer-demultiplexer for transfer of the thirty array channels to ground and the computer controlled RF processing circuits to adaptively form an individual beam for each user. To test and evaluate the system an interference scenario is included consisting of ten interfering user sources, each transmitting a carrier signal PSK modulated by a unique Gold code of length 2047. A desired user simulator will also be built which will enable hardline synchronization tests to be run on the simulation system.

The equipment simulating the satellite components consists of the S-band array, S-band receiver, multiplexer and phase locked frequency source. Layouts for the S-band array have been evaluated by employing the effective area of 2.45λ diameter as the minimum spacing criteria for the elements. For this spacing a 31 element layout of 72 inch diameter and 42 element layout of 84 inch diameter, using triangular symmetry, has been selected as the baseline approach. These diameters are compatible for both the Delta 2419 investigated by Rockwell International** and the expanded Delta under investigation by RCA.

* AIL Division of Cutler-Hammer, "Adaptive Ground Implemented Phased Array" NASA Contract No. NAS-5-22653, February 1973

** Rockwell International, "TDRS Configuration and Tradeoff Study", NASA Contract NAS-5-21705, Part I, Vol. IV, Oct. 1972. Part II, Vol. III, April 1973

Measurements of mutual coupling between antennas indicated that coupling levels exceed -50 dB at spacings over 2λ , and beam distortion is reduced to tolerable level at 2.45λ spacing. Therefore, a diameter greater than the effective diameter previously discussed will be used in the antenna array resulting in an overall diameter of 72" for 31 elements.

The antenna element which has been selected for the array is a bifilar helix wound on a lexan tube. Initial breadboarding of the element yielded a peak gain of 15.5 with an element HPBW of 27° . Since an array gain of 28 dB is required over a 26° FOV, an element gain of 13.2 dB is required at the $+13^\circ$ beam points. The design approach selected has been to maximize the element HPBW so that the 13.2 dB requirement can be obtained with the smallest peak gain. This approach requires a highly efficient element with low sidelobe levels. To achieve these results, improved performance techniques developed during an AIL in-house development study have been applied to the TDRS simulation antenna resulting in 16 dB sidelobe levels at 2287.5 MHz with a HPBW of 30° . The 13.2 dB minimum gain at 26° FOV was exceeded by this device.

A computer analysis was conducted which performed an omniscient solution of a fixed scenario of ten users. The improvement in signal-to-interference was then calculated for six user positions in a typical orbit for both an adaptively formed beam and an antenna array beam simply pointed at the desired user. The analysis assumed relative signal and interference power levels so that the resultant array signal-to-thermal noise ratio would be equivalent to 10 dB and 15 dB for the pointed beam. The results indicated that AGIPA provides more improvement in S/I+N than a pointed beam.

Design of the multiplexer-demultiplexer is based upon performing the main channel isolation filtering at the 1st IF of 150 MHz. Considering phase and amplitude distortion and filter cost and delivery as well as array channel isolation requirements, a 3.75 MHz 3 dB bandwidth, six pole, cavity filter has been selected. The filter will provide 30 dB of rejection at the 6 MHz crossover points between the FDM channels. Chip rates

up to 2.0 Mb/s will be able to function within the $\pm 10^\circ$ phase linearity and $\pm 5^\circ$ phase tracking points contained within the 3.0 MHz filter bandwidth. The filter rejection selected will provide 40 dB of channel isolation which places the crosstalk noise below the thermal noise at the output of the processing correlators of the adaptive array. The distortion effect of higher chip rates on system performance can be evaluated during the test program.

Evaluation of code isolation between the multiple access users and the effect on AGIPA performance has been investigated partially with the original 5 element AGIPA but no analytical or computer simulation models have been established as part of this effort. Some estimates of the relative power levels for a scenario of users have been calculated using order of magnitude estimates for code isolation where the integration period is less than a full code period. For a scenario consisting of 2 users at 100 Kb/s, 3 at 30 Kb/s and 3 at 1 Kb/s, the equivalent interference power for each data bandwidth was calculated. An assumption was made that the 30 dB code isolation provided by the 2047 length Gold code is reduced by the ratio of code lengths to the total number of chips calculated.

The adaptive processor correlates the summed array outputs with individual channel outputs to develop steering signals. Preliminary tests conducted for $S/I = 5$ dB indicated no change in AGIPA performance until interference levels reached $S/I = -10$ dB to -16 dB. For these values the convergence time increased and the nulling capability degraded. Since the adaptive algorithm measures both signal and interference to compute a change in weight, larger amounts of interference can be tolerated in the signal channel as the preliminary tests which were performed suggested. Therefore, it is anticipated that similar performance will be achieved for the thirty element array.

In addition, further improvements such as a coded pilot, omniscient solution, contrived solution and a data cancellation technique APL is investigating can be applied to make the algorithm independent of data rate and therefore code isolation properties.

The equipment is implemented utilizing as many of the components from the previous program as practical. User simulation hardware employs crystal controlled S-band oscillators modulated by a unique Gold code of length either 2047 or 3191. Ten of the S-band modules from the previous AGIPA program are utilized in the receiver. Twenty-two new S-band downconverter modules, employing microstrip preselector/mixers, will be assembled to build thirty operating and two spare channels. The S-band receiver channels are housed in four drawers, each with eight channels, so that expansion to forty channels requires the addition of another drawer for which room has been provided.

The system sensitivity is based upon the 12 dB noise figure of the S-band downconverter. A user and interference model was developed to derive a maximum input signal level of -83 dBm for the system. This signal level will permit a 48 dB dynamic range for test purposes.

Multiplexing is accomplished by initially converting the S-band channels to 150 MHz, filtering the spectrum, and converting the channels in groups of eight to frequencies from 68 MHz to 110 MHz with 6 MHz channel spacing. The four subgroups are then converted to a supergroup frequency placing all the channels within a bandwidth of 271-463 MHz. A phase locked frequency source provides coherent references to develop all the subgroup and supergroup frequencies.

The ground system contains the 32 RF processing channels, where a complex weighting vector is placed on each demultiplexed array channel. The weighting network has been modified and the current implementation takes the form of a vector generator, providing rectangular rather than polar coordinate weighting functions. This simplifies the computer calculations and reduces the step time of the adaptive algorithm. Further improvements in step time will be achieved by means of the floating point processor incorporated into the computer processing.

2.0 SYSTEM DESIGN

2.1 SYSTEM REQUIREMENTS AND DESIGN CONSIDERATIONS

ACCURATE SIMULATION OF THE TDRS S-BAND MULTIPLE ACCESS LINK IS THE PRIMARY OBJECT OF THIS PROGRAM

The design guidelines shown in Table 2-1 which have been employed in the development of a detailed design for the TDRS simulation system are to (1) accurately simulate the interference environment and performance of the multiple access system, (2) build the simulation equipment using components from the previous AGIPA program* wherever possible, and (3) to complete the assembly and test of the hardware so that timely information is available for NASA regarding system performance.

The equipment which will comprise the simulation system is separated and packaged as shown in Figure 2-1, i. e., Scenario Equipment, Satellite Equipment, Ground Equipment. With the overall objective being an RF simulation of the system, the scenario equipment is designed to radiate ten interfering and one desired signal at a nominal center frequency of 2287.5 MHz. Each interference source contains an S-band oscillator, 2047 or 8191 length Gold code generator, so that the sources contain independent carrier frequency running off a common clock which closely approximates the actual situation.

The equipment which will ultimately be contained within the satellite is basically the 30 element array and S-band receiver, containing 30 operating channels with two spares. Multiplexing of the array channels is accomplished in two steps by initially combining groups of 8 array channels in subgroup multiplexers and combining the 4 groups of eight in a supergroup multiplexer.

The signal received at the TDRS on the forward link contains both the data for simulated forward link transmission to a user on 2106.40625 MHz and a pilot for locking the phase locked loop. Coherent frequencies are generated in a phase locked frequency source providing all frequencies for the satellite.

*NAS-5-22 653

TABLE 2-1 OVERALL SYSTEM SPECIFICATIONS

MULTIPLE ACCESS FREQUENCY	2287.5 MHz
DATA RATES	1 Kbps, 10 Kbps, 30 Kbps, 100 Kbps
LINEAR PHASE BANDWIDTH	3.0 MHz
3 dB BANDWIDTH	3.75 MHz
INTERFERENCE SOURCES	10
SIMULATED USER TRANSMITTER	1
ARRAY ELEMENTS	30
ELEMENT GAIN	15.5 dB
ARRAY ELEMENT COVERAGE	+13 DEGREES
NOISE FIGURE	12 dB
(10 FT. CABLE TO MIXER FRONT END)	
MUX-DEMUX CHANNELS	30 OPERATING, 2 SPARE
BEAM FORMING NETWORKS	1
FORWARD LINK FREQUENCY	2106.40625 MHz
CHIP RATE	VARIABLE TO 2 Mbps
CODE LENGTH	2047, 8191 (SELECTABLE)
FREQUENCY TRANSLATION	COHERENT

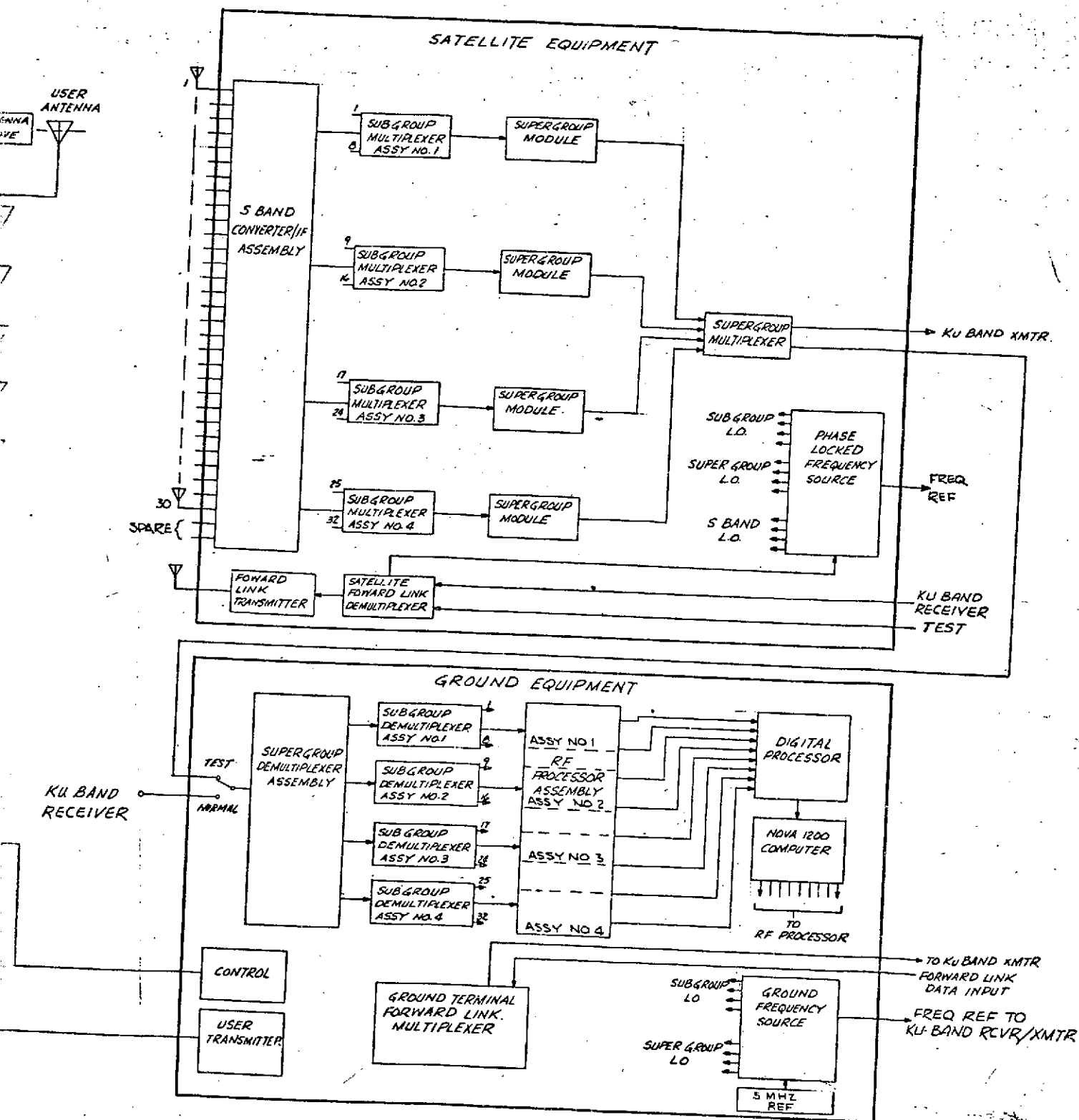
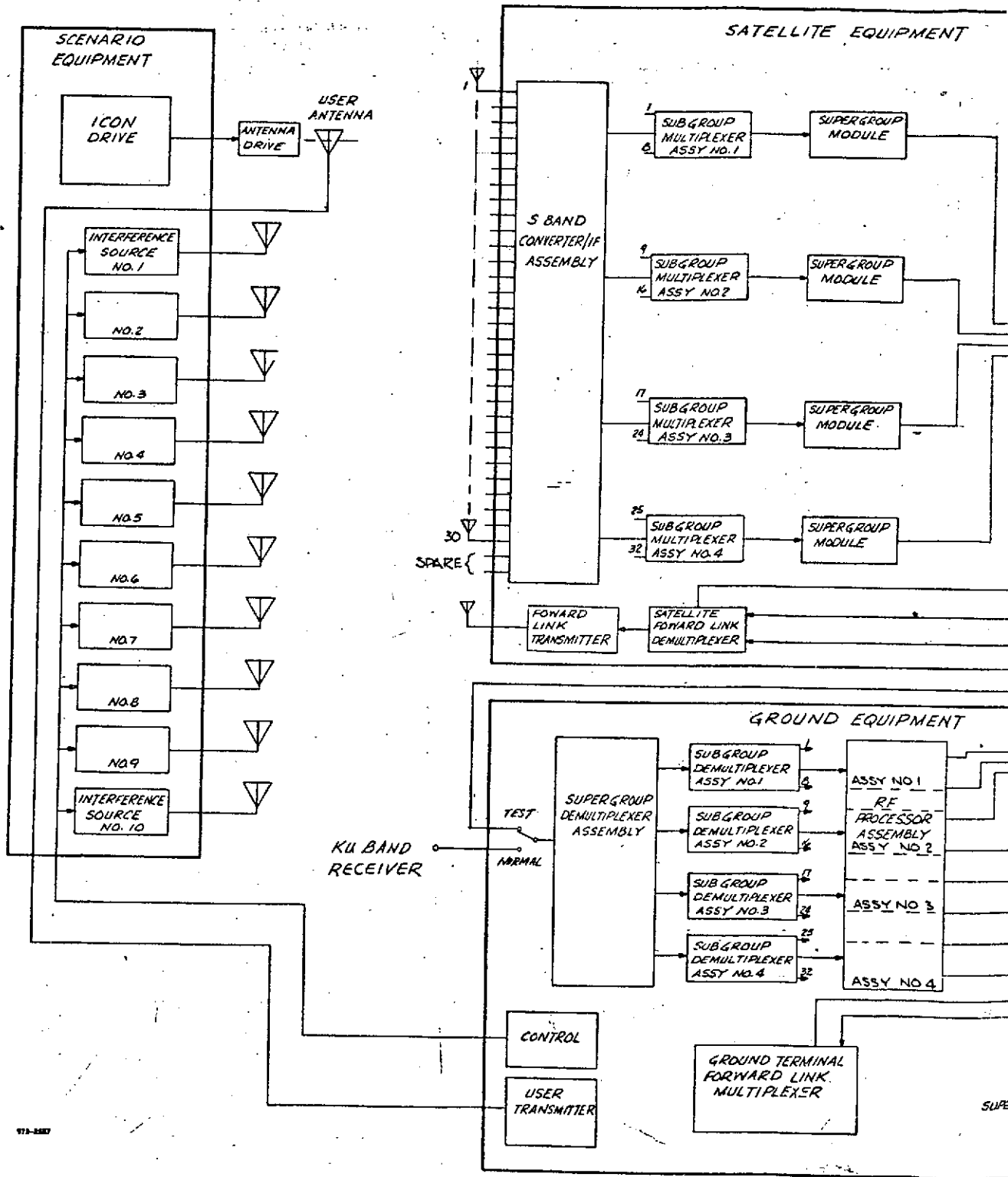


FIGURE 2-1
TDRS SIMULATION SYSTEM



2.1.1 SYSTEM PACKAGING

THE SYSTEM WILL BE REPACKAGED INTO A SET OF FIVE RACKS; SCENARIO SYSTEM, SATELLITE SYSTEM AND GROUND SYSTEM ARE EACH GROUPED SEPARATELY.

The physical configuration of the system, (Fig. 2-2) will consist of 5 equipment racks and a teletype keyboard to provide a computer input/output interface. The first rack of the ground system contains assemblies which are taken almost directly from the previous AGIPA hardware. Modifications include changing the code generator and frequency of the user transmitter (5160), the addition of new controls (5150), and uprating BERT (5120) to handle the 100 Kb/s data rate.

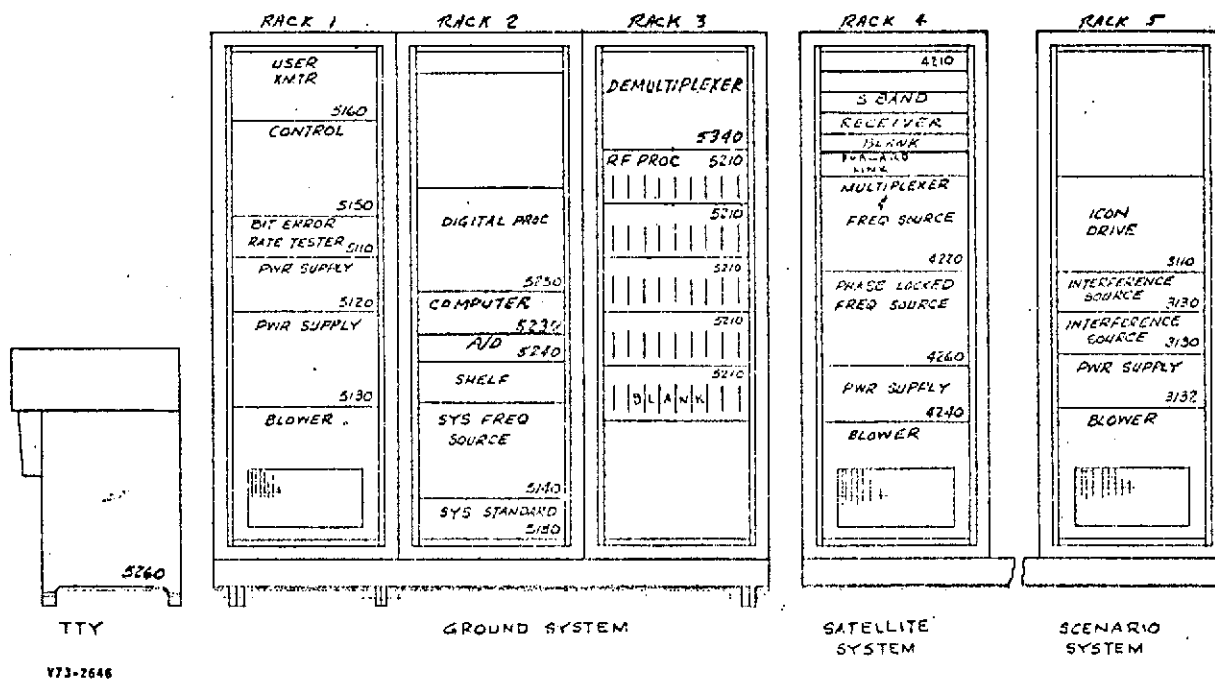
The second rack contains three new drawers, which include the demultiplexer (5340), system frequency source (5140) and the system standard (5180) which is a GFE HP107-BR oscillator. The digital processor (5250) and computer (5230) are modified to handle the four data rates and thirty channels respectively.

The third rack houses the thirty-two RF processing channels. Space has been provided for expansion to forty channels by building four (5210) drawers, each containing eight channels, and leaving space for a fifth drawer. It will be seen that this approach of providing for the addition of eight channels is carried throughout the entire system design. For example, five-way power dividers ($5 \times 8 = 40$) are used for L.O. lines rather than four-way.

The satellite system in rack 4 contains four new assemblies and utilizes a substantial portion of the existing hardware. The S-band receiver (4210) will contain the ten original downconverter modules - twenty-two new S-band down converters, and IF amplifiers for each of the thirty-two channels. The multiplexer (4220) is a new design. Most of the components in the PLL frequency source (4260) will be taken from the existing source and with modification will generate the required frequencies.

Size and power requirements of the simulated satellite and ground systems will not be truly representative of the actual hardware. This approach was selected in order to minimize costs through the use of off-the-shelf components and to meet the rapid delivery requirements.

FIGURE 2-2
TDRS SIMULATION SYSTEM PACKAGING



The fifth rack contains the drive electronics for the user antenna (3110) and the interference sources (3130). The center frequency of the ten existing S-band oscillators will be modified and a code generator and PSK modulator added to each to simulate the interfering users.

2.2 ARRAY ANTENNA DESIGN

PAYLOAD LAUNCH CAPABILITY OF THE EXISTING DELTA 2914 LIMITS THE NUMBER OF ANTENNA ELEMENTS TO 31 IN A 72 INCH DIAMETER, WHILE DOWNLINK FREQUENCY SPECTRUM AVAILABILITY AND SIZE LIMIT THE EXPANDED DELTA TO 40 AGIPA CHANNELS AND 2 TRANSMIT CHANNELS IN AN 84 INCH DIAMETER CONFIGURATION.

The design areas of the antenna segment of the AGIPA system include the layout of the array, the configuration of the antenna element and an analysis of the system performance.

The performance analysis utilizes a computer simulation of the selected array layouts operating in an interference scenario. In performing the antenna design several constraints and guidelines are employed in arriving at the selected configuration. These constraints are:

- The size and weight carrying capability of the Delta 2914 launch vehicle and the potential utilization of an expanded capacity Delta launch vehicle currently under development.
- Providing the maximum array antenna gain over a $\pm 13^\circ$ FOV.
- Selection of an implementation approach which falls within the cost and schedule requirements of this program.

The first criterion, the launch vehicle, has been extensively studied for NASA* by Rockwell International and for the existing Delta 2914 shroud (96 inches in diameter), a payload diameter of 84 inches has been identified, permitting a 2 inch clearance for dynamic payload motion. Also, an array configuration of thirty

*Rockwell International, "TDRS Configuration and Tradeoff Study" NASA Contract No. NAS-5-21705, Part I, Vol. IV, October 1972; Part II, Vol. III, April 1973.

receive elements and one transmit element was selected based upon the weight and power which the spacecraft could support. The thirty-one elements are contained within a diameter of 72 inches.

As previously mentioned, further evaluation of the Delta 2914 vehicle has indicated that an array diameter of up to 84 inches is possible with cutouts for the high gain antennas and solar panel deployment arms. Therefore, the 72 inch diameter and 84 inch diameter have been configured for 31 element and 42 element arrays respectively to study the performance of both systems. The thirty-one element AGIPA is compatible with the existing Delta 2914, while the forty-two element AGIPA (40 receive-2 transmit) is representative of a system which could be installed on an expanded Delta currently under evaluation by RCA.* The expanded Delta will provide the launch capability for the eleven additional channels.

A second limitation on the number of AGIPA channels is the availability of spectrum on the TDRS to ground link. Since only 240 MHz of the downlink K_u -band spectrum can be devoted to AGIPA, and since a channel spacing of 6 MHz is required, a maximum of forty active channels could be used. Thus, should more spacecraft payload capability be made available, the AGIPA system would still be limited to forty receive channels.

Finally, this program is based upon implementation of a 30 channel AGIPA system. Array configurations with 30 active elements and 12 terminated elements have been considered for the purpose of evaluating the performance of a more tightly packaged layout. We have, however, elected to employ the 30 element configuration and consider implementation of the 40 element array for a later program should the expanded Delta approach become the baseline vehicle.

*Conversation with Len Deerkoski, NASA/GSFC

2.2.1 ELEMENT REQUIREMENT

FOR AN ARRAY GAIN OF 28 DB OVER A $+13^\circ$ FOV, AN ELEMENT PEAK GAIN OF 16.2 DB IS REQUIRED WITH AN EFFICIENCY FACTOR OF 28, 180. THE SELECTED APPROACH IS AN ELEMENT GAIN OF 15.5 DB WITH AN EFFICIENCY FACTOR OF MORE THAN 30,000 TO MEET THE ARRAY REQUIREMENT.

The design of an element for the array has to satisfy the system design goal of 28 dB antenna gain over a $+13^\circ$ FOV. To provide high element gain and wide coverage, the antenna element must have a large gain-beamwidth squared product expressed as,

$$G_{el} = E/(\text{HPBW})^2$$

where,

E is the beamwidth efficiency factor as related to the number of square degrees in a sphere

The element requirement necessary to provide 28 dB of array gain can be expressed as:

$$G_{el}(+13^\circ) = G_A(+13^\circ)/N$$

where, N is the number of elements.

For a thirty element array, the element gain required at the $+13^\circ$ point is 12.2 dB. Shown in Figure 2-3 is a plot of peak gain versus HPBW. Also plotted are the results achieved with several hardware implementations. The family of curves for lower efficiency factors are more representative of practical implementation and 25,000 has been the limit of past development programs. An AIL in-house IR&D program has yielded greater than 30,000 and the techniques developed therein will be incorporated in the design.

Since the element pattern has an approximate parabolic shape, the gain can be expressed as,

$$G_{\text{peak}}^{(0)} = \frac{G_{EL}(+13^\circ)}{\left[1 - 0.293 \left(\frac{2\theta}{\text{HPBW}}\right)^2\right]^2}$$

- (4) NASA, NIMBUS ANTENNA, 1971
- (3) AIL, DRS ANTENNA, 1970, NAL-5-10589
- (2) TDRS BREADBOARD, NOV 1973
- (1) AIL IN-HOUSE IRFD, JAN. 1974

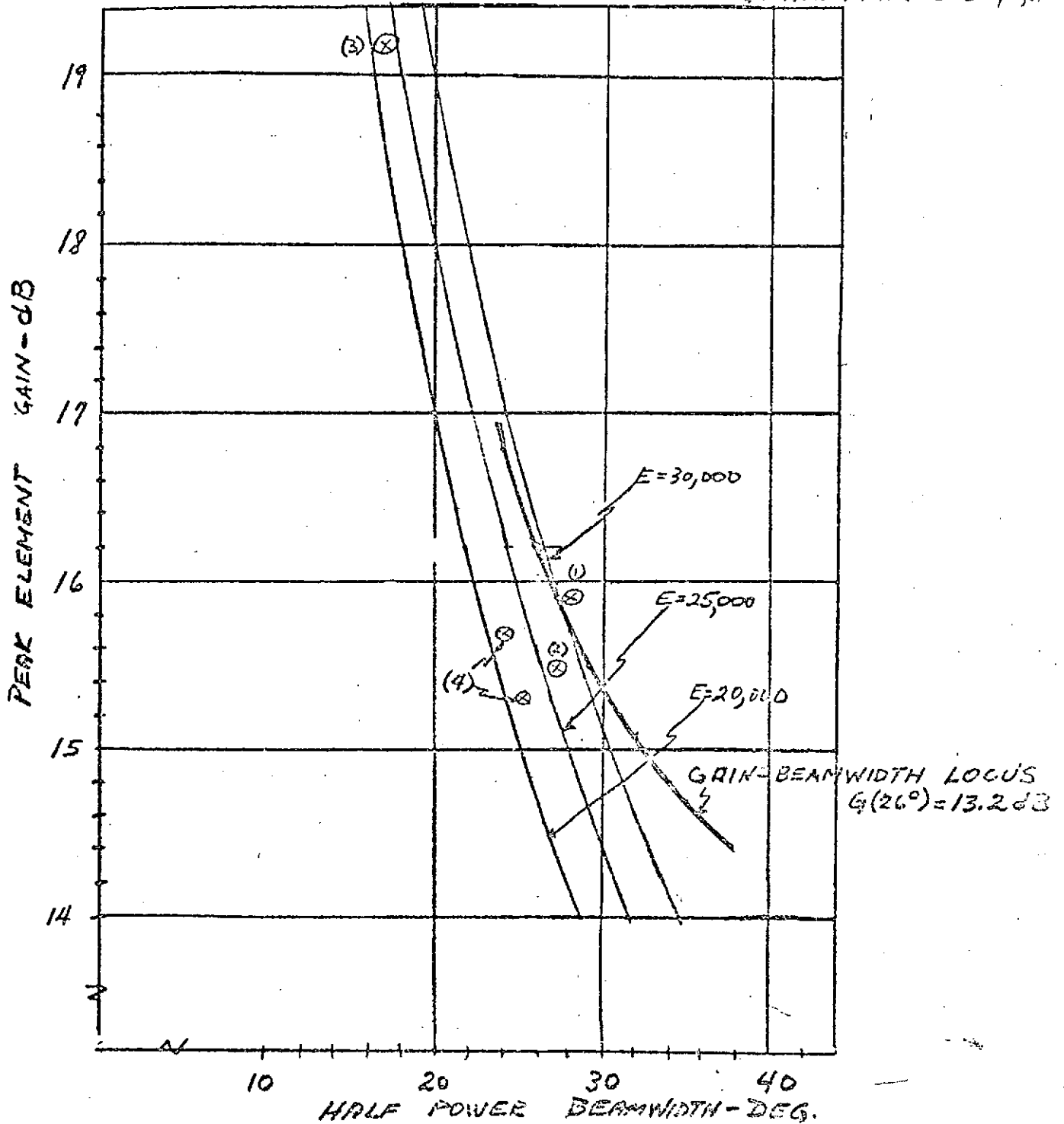


FIGURE 2-3
ELEMENT GAIN VS. HPBW

Therefore, for an element HPBW of greater than $+13^{\circ}$, which is representative of elements (1) and (2), the peak gain requirement is reduced while the element still provides a minimum gain of 13.2 dB over the 26° FOV. The above equation has been plotted in Figure 2-3 as a function of HPBW for a constant element gain of 13.2 dB at the 26° FOV point. This curve shows the range of peak gain and HPBW which would meet the minimum array gain requirement.

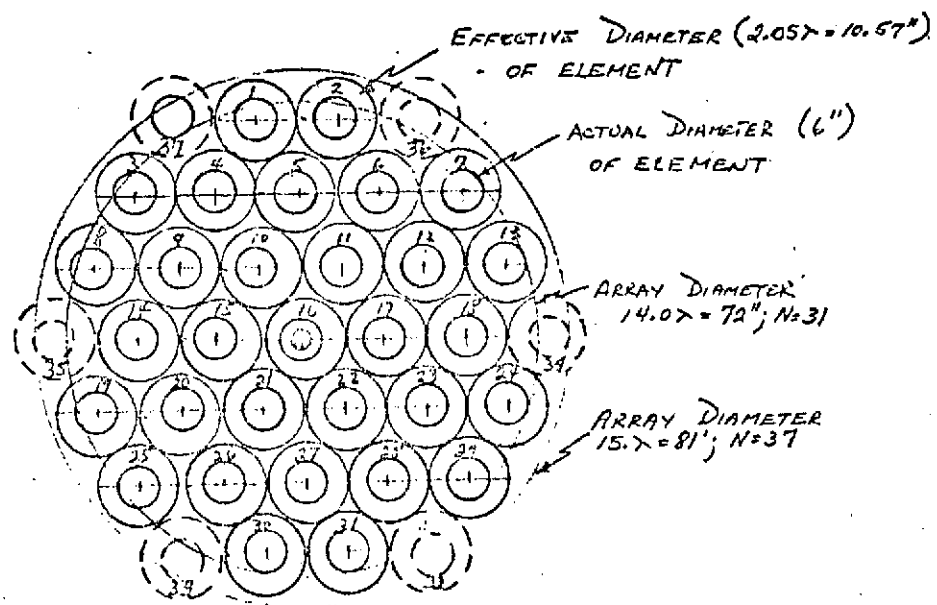
2.2.2 ARRAY LAYOUT

TRIANGULAR SYMMETRY IS SELECTED FOR THE THIRTY-ONE ELEMENT ARRAY RESULTING IN A 72 INCH DIAMETER FOR 15.5 DBI ELEMENTS.

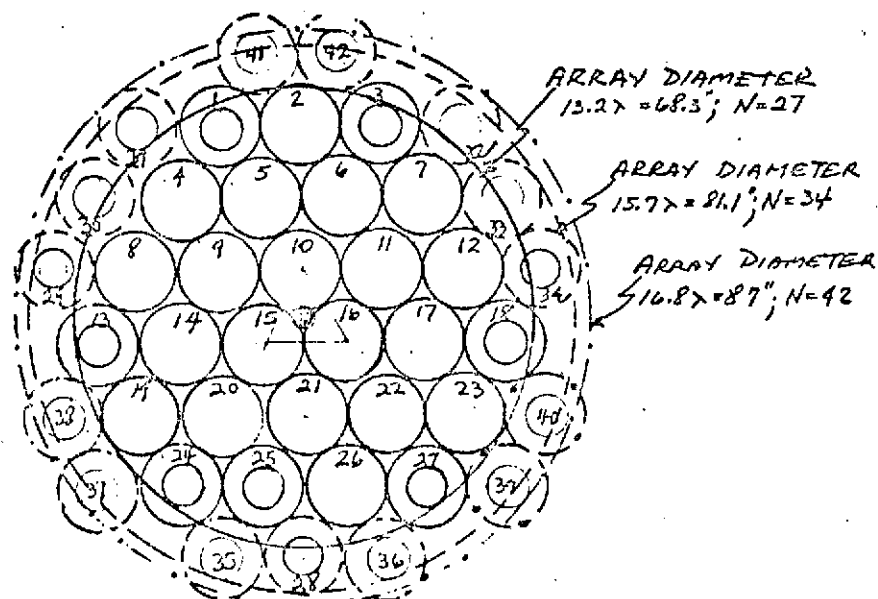
In the layouts of the array elements, several key guidelines used are:

- Adjacent elements are conservatively spaced such that their effective areas ($A_e = \frac{\lambda^2 G_{el}}{4\pi}$) are contiguous (touching) but do not overlap. This is an empirically verified approximation that is commonly used to minimize mutual coupling and to insure sufficient isolation between adjacent elements (and receive channels). It is to be noted, however, that tests are currently in progress which measure the actual spacing that can be used between adjacent helix elements with gains of approximately 15.5 dBi. The tests proved that 2.45 λ spacing is required to prevent element pattern degradation.
- Adjacent elements are arranged in a triangular format for maximum packing density.
- Prime consideration is given to the 31-element array; however, growth considerations have been included for up to 40 receive elements.

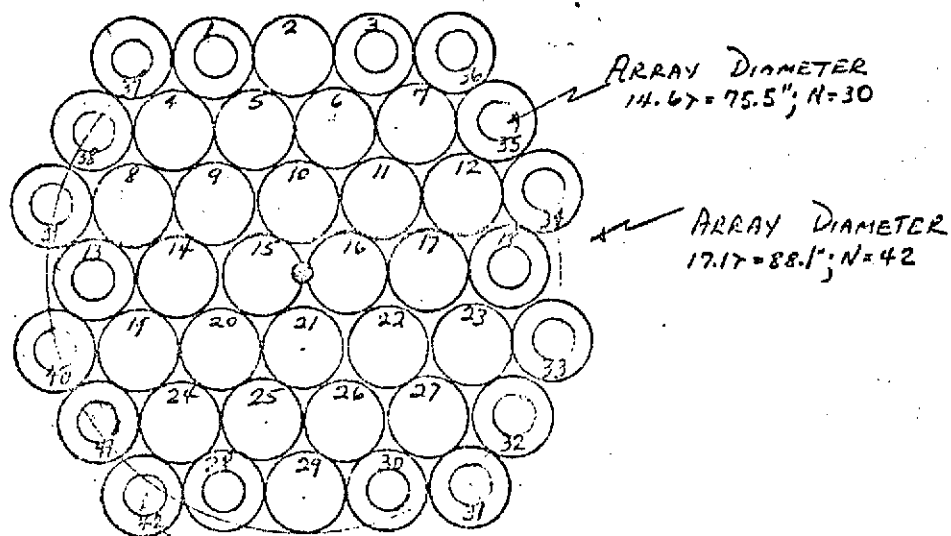
Four typical array layouts have been considered as illustrated in Figure 2-4. The first three layouts have hexagonal symmetry whereas the fourth figure has circular symmetry. In each of the figures, the effective areas of each element are shown touching but not overlapping. In the outer periphery, the actual element diameters are laid out adjacent to the minimum array diameter (D_{min}) since the physical diameter for a helix element is less than its effective diameter. In addition, by placing the peripheral elements equidistant from the center, the array performance characteristics will be more uniform when the beam is scanned in any direction. The concentric circles represent D_{min} required for N array elements.



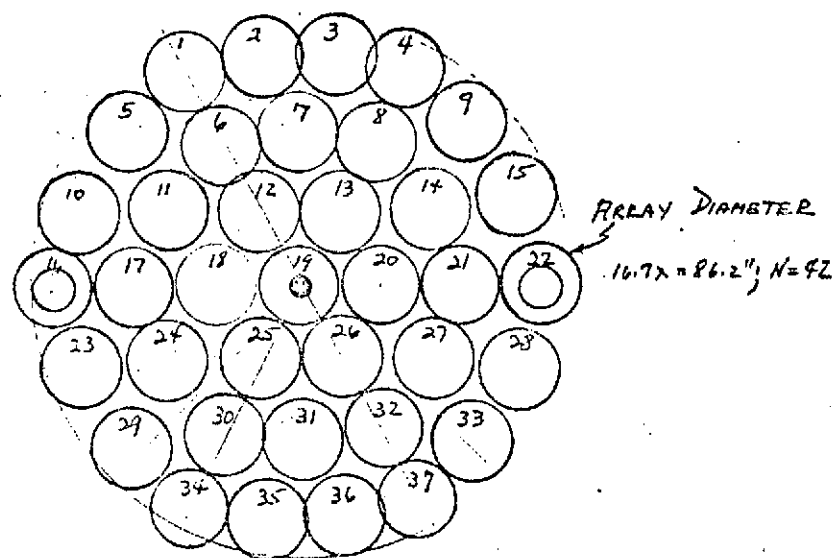
CONFIGURATION A



CONFIGURATION C



CONFIGURATION B



CONFIGURATION D

FIGURE 2-4

ARRAY LAYOUTS FOR EFFECTIVE AREA TRACKING

The preferred layout is shown in configuration A and provides the most compact layout for the required 31 elements.

For element gain of 15.5 dBi, its d_{eff} is estimated at 2.45λ ; and D_{min} is 14.0λ or 72 inches.

Also shown in the various layouts are arrays of 27 to 42 elements. All four layouts provide practical array configurations for larger number of elements. Configurations A and D present symmetrical 37 element arrays; configurations B and C show possible 42 element arrays, required D_{min} of approximately 88.1" and 87". The 42 element array is attractive since it can provide 40 elements for receive only, and 2 separate elements for transmit. Of these layouts, configuration A is selected as the preferred configuration for 31 elements due to its symmetrical element location. This layout provides optical clearance for the two horizon sensors and the four structural arms supporting the two high gain reflectors and the two solar array panels.

The preferred layout for the 42 element array is configuration B but this layout is larger than the 84 maximum diameter previously identified. With some overlap of element aperture the array diameter can be reduced with some degradation of performance.

2.2.3 S-BAND ANTENNA ELEMENT

BIFILAR HELICAL ELEMENT SELECTED FOR ARRAY ELEMENT

A bifilar helical element designed to operate over 2.2 GHz to 2.3 GHz has been selected for the TDRS Multiple Access S-band array. The bifilar design has been shown in empirical test measurements to provide a gain improvement of approximately 3/4 dB over a single filament type.

The element design is illustrated in Figure 2-5 and employs a 21-1/8" bifilar helical radiating structure wound on a 1-1/2" OD lexan tubing. A 1/8" copper tape with non-conductive adhesive coating on one side (manufacturer - 3M) is used for the helical windings. The bifilar wound filaments are fed with a microstrip balun and matching network printed on a thin teflon glass disc located at the base of the support tube. The microstrip network is centrally fed with a type N bulkhead connector. The bifilar helical tube assembly as well as the microstrip network are sprayed with clear krylon paint for protection against moisture and/or copper oxidation.

Test data were taken in an anechoic chamber over 2.2 to 2.3 GHz frequency band. Typical linearly polarized radiation patterns taken at the 2.2875 GHz operating frequency are shown in Figure 2-6. The patterns typically illustrate the broad beam and low side lobe levels that have been achieved. The design provides peak gain achieved at 2.2875 GHz of 15.5 dBi, and its relatively broad beams of approximately 30° at the half power beamwidth (HPBW) points provide gains at $\pm 13^\circ$ scan limits of 13.3 dBi. As a result this bifilar element provides a 30 element array gain of 28.0 dBi as required.

Table 2-2 summarizes the results of the VSWR, HPBW, side-lobe level, axial ratio and gain measurements taken over the entire 2.2 to 2.3 GHz frequency band. The table also shows the computed gain-beamwidth squared product ($G \times \text{HPBW}^2$) which, as previously explained, is a convenient figure of merit to evaluate electronically scanning antenna designs.

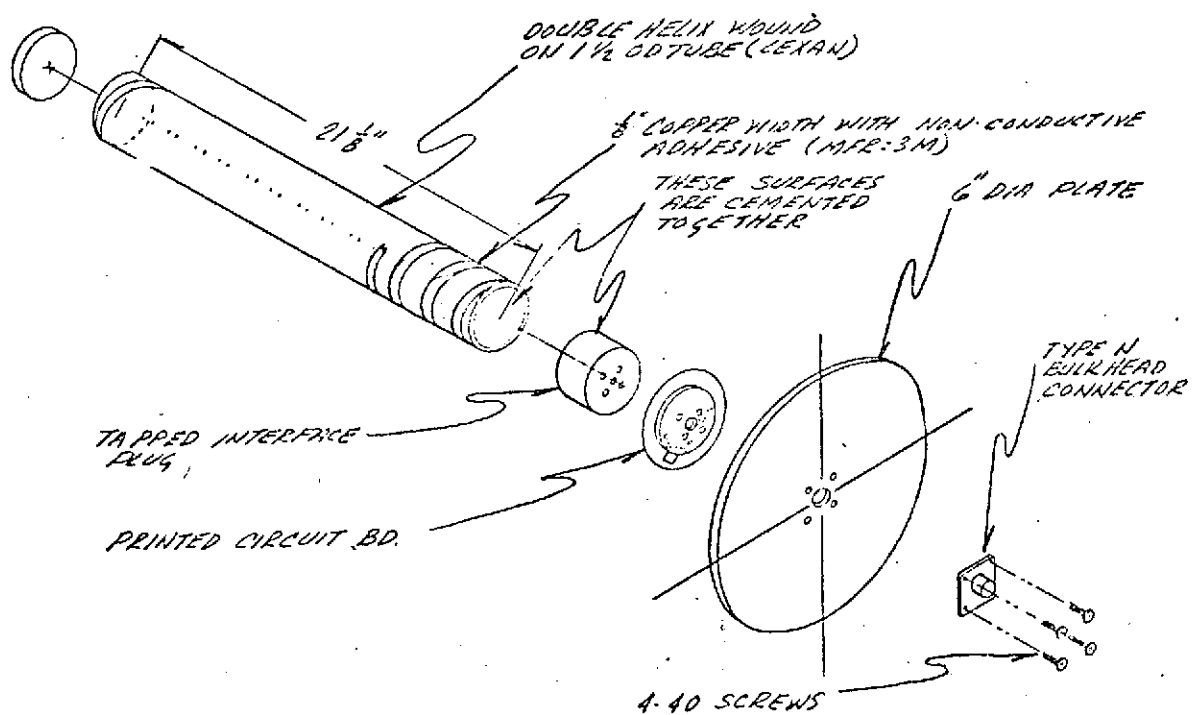


FIGURE 2-5
ANTENNA ELEMENT DESIGN

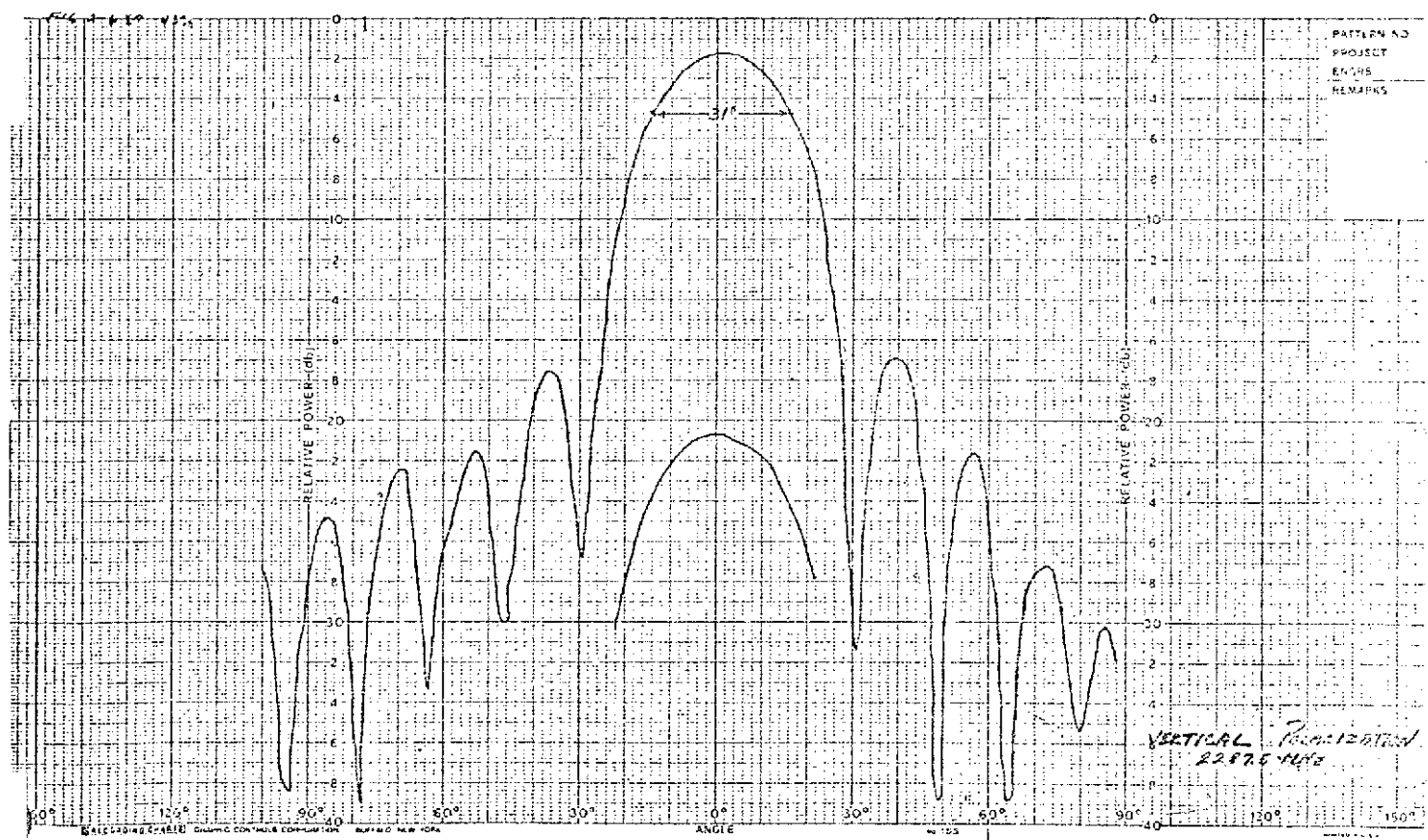


FIGURE 2-6
LINEARLY POLARIZED RADIATION PATTERNS
FOR BIFILAR HELIX ELEMENT

TABLE 2-2

SUMMARY OF BIFILAR HELICAL ELEMENT PERFORMANCE

PARAMETER	FREQUENCY IN GHz			
	2.2	2.25	2.2875	2.3
VSWR	1.20:1	1.08:1	1.16:1	1.03:1
HPBW-VP	33	31	31	31
HP	30	30	29	31
SIDELobe (dB)-VD	15.5	14.6	15.0	14.3
HP	15.0	19.0	17.5	19.2
AXIAL RATIO (dB)	0.4	0.4	0.6	0.6
GAIN (dBi)				
o at 0°	15.7	16.0	15.5	15.2
o at 113° (VP)	13.9	14.1	13.4	13.2
o at 113° (HP)	13.6	13.8	13.3	12.8
GX (HPBW) ²	36,800	37,100	31,800	29,800

Mutual coupling measurements were also taken employing two bifilar helical elements varying the element center-to-center spacing from 1.2, 1.45, 2.0, 2.4 and 3.8 λ . Radiation patterns, gains and isolation (transmit into one element and measure leakage into adjacent element) data were measured over the 2.2 GHz to 2.3 GHz band. Measured data showed that considerable coupling occurs at the closer spacings, and that a minimum spacing of approximately 2.4 λ is required to minimize mutual coupling effects, and to preserve the individual element performances shown in Table 2-2 and Figure 2-6. The measured isolation at the required 2.2875 GHz operating frequency for this spacing is 54 dB.

2.2.4 CALCULATED ARRAY PERFORMANCE

A SCENARIO CONSISTING OF NINE INTERFERENCE EMITTERS AND ONE DESIRED SIGNAL IN A 26° INCLINED ORBIT IS SELECTED TO EVALUATE 1 KB/S AND 100 KB/S ARRAY PERFORMANCE.

Typical array patterns were computed for the 31 element array and 42 element array. In both cases adaptive three dimensional radiation patterns in a jamming environment were generated showing the AGIPA performance.

The jammers are assumed to be intentional signals emitted by other in-band S-band multiple access users. The scenario shown in Figure 2-7 has been used to evaluate the adaptive array performance. Ten multiple access users are assumed to be within the total $+13^{\circ}$ FOV of the S-band array; however, only 3 of these users are assumed to be within the main beam of the array at any one time; one desired and two interfering users. Of these 10 users, 2 are 100 Kbps, 3 are 30 Kbps, 2 are 10 Kbps and 3 are 1 Kbps users; therefore, the power received from these users can vary as much as 20 dB. The worst case interference environment is a 1 Kb/s desired user, versus two 100 Kb/s interference users in the main beam with the remaining 7 interference emitters located outside the main beam. This worst case can represent nearly 23 dB difference in the received signal-to-interference plus noise ratio in the desired and interference channels. Conversely, the best case occurs when the desired user is transmitting 100 Kbps and two interference emitters in the main beam are transmitting 1 Kbps; the remaining 7 interference users are outside the main beam.

In the selected scenario, it has been assumed that the desired user is moving in a 26° inclined orbit with a background of 9 fixed interfering emitters. The adaptive patterns are computed at the 6 locations indicated along this path, to illustrate the array performance through a typical orbit. It is to be noted, however, that at any given desired user location that only two interference emitters occur in the main beam of the S-band array. These two emitters are placed within the HPBW and/or outside the HPBW but always within the main beam, and are also selected to provide several combinations and

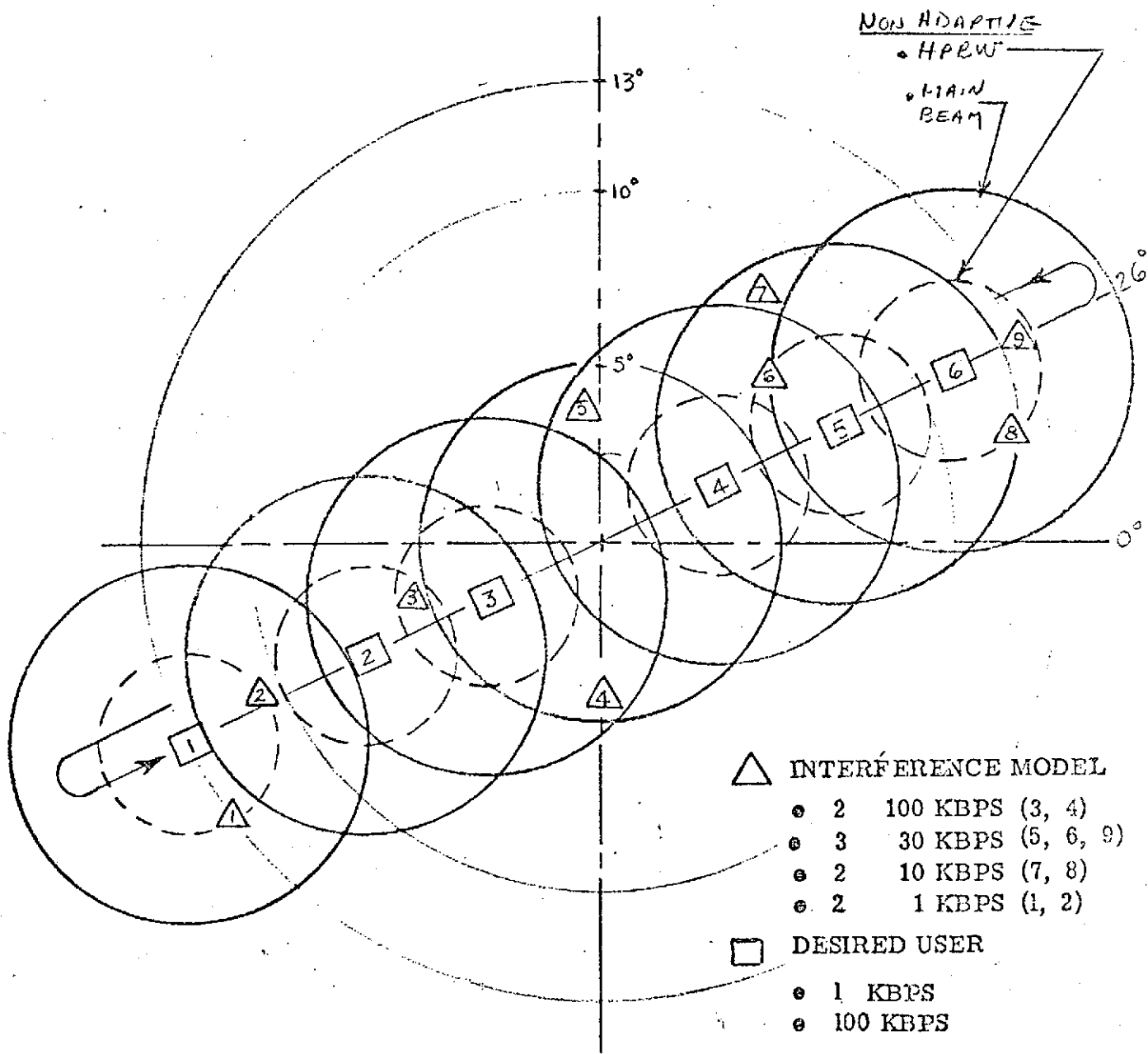


FIGURE 2-7
TYPICAL SCENARIO

distributions of 1 to 100 Kbps users in the main beam which realistically simulates the interference environment that will occur in operation.

A second case was also examined where the desired user was a 100 Kb/s user; using the same scenario shown except that the data rate for the desired user has been interchanged with jammer #3.

2.2.5 PERFORMANCE OF THIRTY-ONE ELEMENT ARRAY

COMPUTER GENERATED OMNISCIENT SOLUTIONS OF THE INTERFERENCE SCENARIO SHOW THAT THE ADAPTIVE ARRAY PROVIDES IMPROVED PERFORMANCE OVER A POINTED BEAM.

To evaluate the performance of the selected 31 element configuration, a computed solution using known user and interference positions and power levels as derived from the previous scenario is presented. This information is arranged in a matrix which derives the optimum weight settings for each element of the array. The resultant $S/I+N$ ratio is then calculated for each of the six user positions. The omniscient solution represents the ideal adaptive solution for each user position and a set of curves is presented comparing the adaptive beam performance to that of simply pointing the beam at the desired user. Figure 2-8 illustrates the performance of the adapted and pointed beam for the 1 Kb/s user. Improvements of up to 17 dB are shown to a minimum of 8 dB.

For the 100 Kb/s case, user (4) in Figure 2-7 was changed to 1 Kb/s and the desired made 100 Kb/s. The curve in Figure 2-9 shows the 100 Kb/s comparison. It can be seen that a significant improvement is achieved for the adaptive system only when the 100 Kb/s user is between positions (2) and (3) where the interfering 100 Kb/s is within the HPBW of the array. This occurs because the other interfering sources are below or near the noise level in the 100 Kb/s user situation. Therefore, a relatively small amount of nulling takes place. Clearly, however, the adaptive concept will always provide either a significant advantage or at least equivalent performance to the pointed beam system.

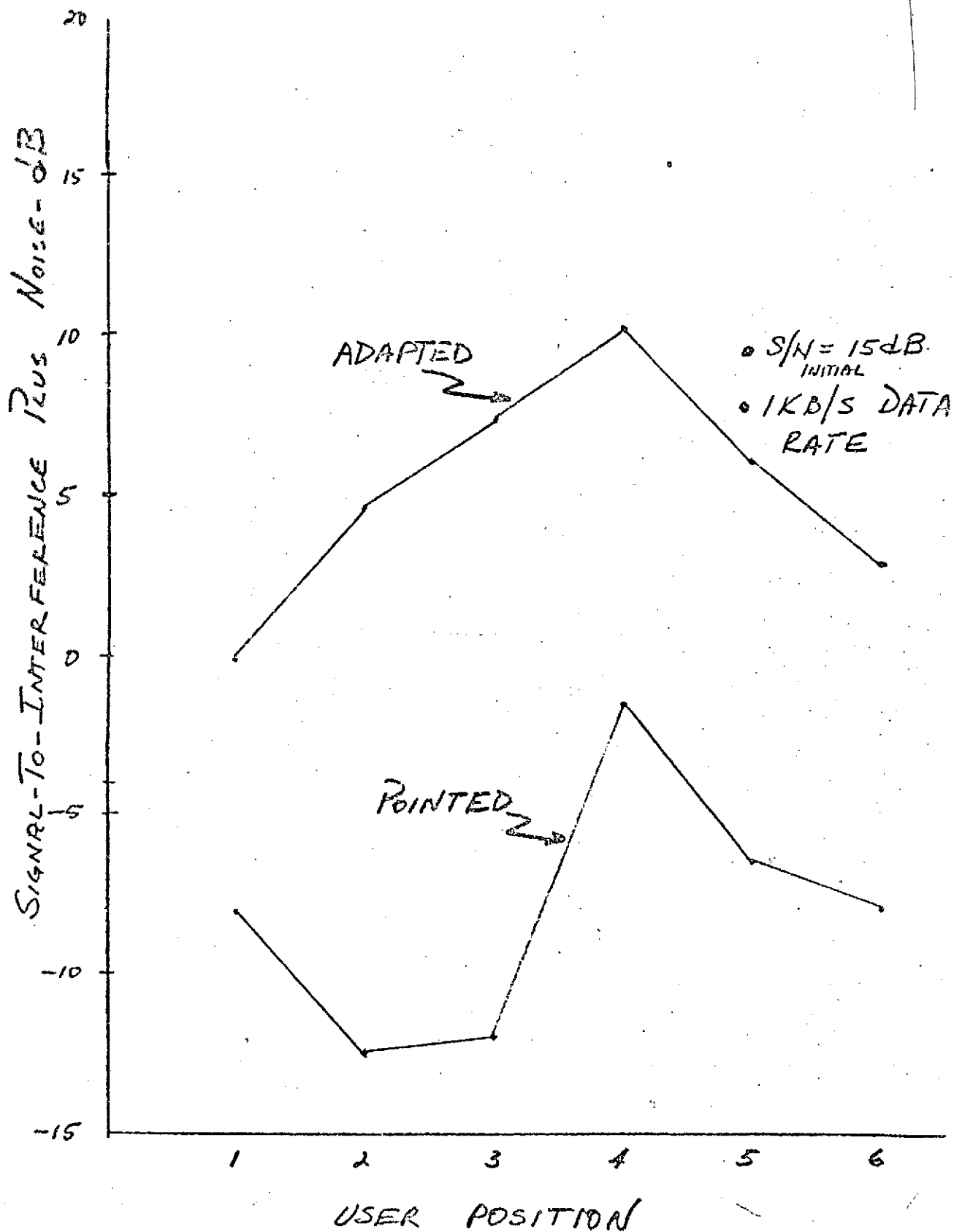


FIGURE 2-8
COMPARISON OF ADAPTED ARRAY VERSUS POINTED
BEAM FOR 1 KB/S USER

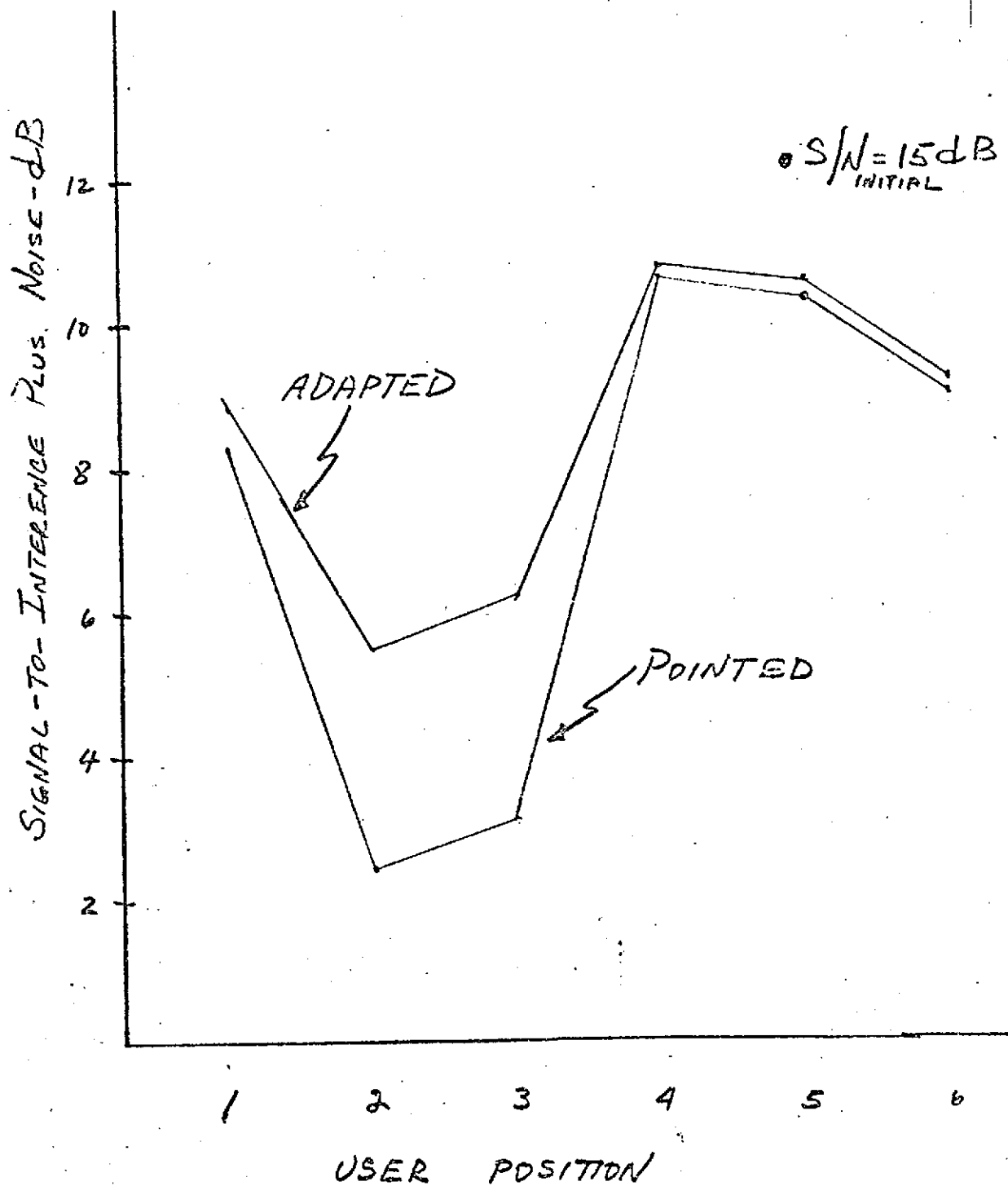


FIGURE 2-9
COMPARISON OF ADAPTED ARRAY VERSUS
POINTED BEAM FOR 100 KB/S USER

2.3 SYSTEM SENSITIVITY

SIMULATION SYSTEM SIGNAL THRESHOLD DEFINED AS A FUNCTION OF SYSTEM DESIGN. THRESHOLD LEVELS FOR EXPECTED DATA RATES COMPUTED FOR THE SIMULATED S-BAND SYSTEM INCLUDING REALISTIC LOSSES DUE TO ELEMENT RECEIVER CABLING.

The sensitivity analysis of the multiple access TDRS simulation system is based upon the S-band receiver input noise figure, the system losses and receiver amplifier gains and noise figures. The system noise figure measured at the input terminal of the satellite receiver rack is designed to be less than 12 dB.

Figure 2-10 shows the receiver noise model and includes a conservative tabulation of the component parameters including gains (positive or negative) and individual noise figures. The noise figures for passive devices have been assumed to be equal to the attenuation of the devices. The S-band downconverter assembly has a noise figure of less than 11.5 dB with its self-contained RF preselector filter, mixer and IF preamplifier. The total contribution to the system noise figure, due to succeeding stages, is seen to be less than .01 dB even for the attenuator set to its maximum loss of 21 dB and allowing for a 3 dB cable loss between the receiver and multiplexer.

The final installation of the system includes a length of coaxial cable between the antenna and receiver rack input. The length of this cable has not been specified but if, for example, a 25 foot length of RG-9 coaxial cable were installed between the antenna and the receiver input terminal, an additional insertion loss of 4.5 dB would be incurred. A system noise model is shown in Figure 2-10 for such an installation. The resultant system noise figure with 25 feet of cable would be approximately 16.3 dB with less than .03 dB contribution due to any of the stages after the downconverter.

In the following analysis the system thresholds are derived exclusive of cable loss. Assuming the noise temperature of the antenna is a nominal 290°K, the available thermal noise power density is -174 dBm/Hz. The system threshold can therefore be evaluated as shown in Table 2-3 for the four operating data rates.

	S-BAND RECEIVER					MULTIPLEXER	
	Pre-Select. Filter	S-band Down Converter	IF BP Filter	IF Amp	Cable & Device Loss	Mixer	IF Amp
Gain (dB)		+33	-8.0	+50	-6.0	-8.0	33
Noise Figure (dB)(or equivalent)		11.5	8.0	5.0	6.0	8.0	5.0
Gain		1995	.1585	10,000	.003981	.1585	1995
Noise Figure (or equivalent)		14.125	6.310	3.162	251.186	6.310	3.162
Noise Figure Contribution per Stage		14.125	2.661×10^{-3}	6.838×10^{-3}	3.982×10^{-4}	2.513×10^{-3}	7.944×10^{-3}
Cumulative System Noise Figure		14.125	14.128	14.134	14.135	14.137	14.145
Cumulative System Noise Figure (dB)		11.50	11.50	11.50	11.50	11.50	11.50

SYSTEM INTERFACE NOISE MODEL

FIGURE 2-10

To achieve a final system bit error rate of 10^{-5} for differentially coherent PSK detection, a carrier-to-noise ratio (E/N_0) of 9.9 dB is required. The detection of the received PSK data will utilize matched filter techniques. The receiver sensitivity threshold, therefore, includes a factor determined by the optimum bandwidth matched to the operating data rate as shown in Table 2-3.

The thirty element phased array provides an array factor gain of 14.77 dB. The input noise figure of the S-band downconverter in the satellite receiver is 11.5 dB. Allowing .5 dB for an inter-connecting cable to the satellite rack input, the total noise figure at the system input terminal is 12 dB. An additional one dB is allowed for the tandem link loss plus one dB for detection loss. The summation of all these factors results in the system noise threshold shown in the last column of Table 2-3 for each of the operating data rates.

TABLE 2-3

SYSTEM THRESHOLD CALCULATIONS						
H (KHz)	Req'd E/N_0 (dB)	BW Reduction (dB)	Array Gain (dB)	Noise Figure (dB)	Tandem Link & Detect. Loss(dB)	Threshold (dBm)
1	9.9	30.0	14.77	12	2	-134.87
10	9.9	40.0	14.77	12	2	-124.87
30	9.9	44.8	14.77	12	2	-120.07
100	9.9	50	14.77	12	2	-114.87

2.3.1 DYNAMIC RANGE

SYSTEM DYNAMIC RANGE DESIGNED TO ACCOMODATE WORST-CASE INTERFERENCE MODEL. ASSUMING UP TO TEN OTHER USERS AT DIFFERENT DATA RATES AS REPRESENTATIVE OF THE INTERFERENCE SCENARIO EXPECTED, A WORST-CASE MODEL IS INCORPORATED INTO THE SYSTEM DESIGN CONSIDERATIONS.

The worst case system environment model assumes, in addition to a desired user at a 100 Kbps data rate, a distribution of ten undesired users at the various system data rates. For each of the eleven users as shown in Table 2-4, the worst case system threshold is given by the summation of the individual noise powers. This is equivalent to -108.87 dBm for the system operating at 100 Kbps.

TABLE 2-4

CALCULATIONS OF MAXIMUM INPUT LEVEL

User Data Rate (Kbps)	Threshold (dBm)	(mw)	No. of Users	Noise/Data Rate (mw)
1	-134.87	3.258×10^{-14}	3	9.775×10^{-14}
10	-124.87	3.258×10^{-13}	2	6.517×10^{-13}
30	-120.87	8.185×10^{-13}	3	2.455×10^{-12}
100	-114.87	3.258×10^{-12}	3*	9.775×10^{-12}

TOTAL NOISE POWER = $1.298 \times 10^{-11} = -108.87 \text{ dBm}$

*Includes one desired user plus two undesired users.

Allowing for a system operating margin of 10 dB, the required rms signal level is -98.87 dBm. Assuming that the combined spectrum of the total signal is Gaussian, the maximum peak signal will increase by an additional 12 dB no more than .01% of the time. A conservative estimate of the maximum peak signal would therefore be -86.87 dBm.

Since the minimum signal or noise threshold for a 100 Kbps data rate is -134.87 dBm, the dynamic range must be made equal to 48 dBm or greater as shown below.

$$\begin{array}{rcl} -86.87 \text{ dBm} & = & \text{peak signal} \\ -134.87 \text{ dBm} & = & \text{threshold} \\ \hline 48.00 \text{ dB} & = & \text{dynamic range} \end{array}$$

Factors that would adversely affect the achievement of this number would be an inadequate linear range of any single component in the complex chain from array element at the TDRS to the eventual data detection at the ground station.

The non-linearities that may occur in the system are due to several different factors. Within each channel the most significant contributions are due, first, to non-linear gain characteristics at high signal levels requiring various components to operate nearer to their saturation levels. In addition, the presence of multiple signals (or noise plus the desired signal) at high signal levels can cause intermodulation distortion products because of the non-linear characteristics of various components at these levels. Any such non-linearities throughout the "receiver-multiplexer-demultiplexer-link-RF processor" chain will determine how faithfully each signal is reproduced. Channel variations in amplitude and phase tracking across the frequency passband will limit the degree of matching between channels.

For a system data bandwidth of 2.25 MHz, and a noise figure of 12 dB, the channel noise threshold is -98.4 dBm. The maximum rms signal level calculated previously is given as -98.87 dBm. The summation of these two power levels equals a total power of -95.6 dBm, or conservatively, -95 dBm. Allowing for the 12 dB

margin, a maximum peak power level of -83 dBm must be accommodated by the system. In evaluating the system for this input power, the power levels at each stage were designed to always be more than 3 dB below the 1 dB compression point even with all gain adjustments set to maximum.

2.4 MULTIPLEXER-DEMULTIPLEXER TRADEOFF

2.4.1 PROBLEM DEFINITION

A MULTIPLEXING APPROACH USING FOUR SUBGROUP AND A SUPERGROUP FREQUENCY CONVERSION WITH A FIRST IF OF 150 MHZ SELECTED. THIS RESULTS IN MAXIMUM UTILIZATION OF EXISTING COMPONENTS AND A DESIGN CONCEPT SUITABLE FOR THE SIMULATION AND ACTUAL FLIGHT SYSTEM.

The multiplexing concept for the S-band multiple access array consists of processing the output of each element of the array such that the channels can be stacked side by side in frequency and transmitted to the ground station via the K_u -band link. At the ground station an inverse process takes place in which the 32* channels of the array are demultiplexed, returning each channel to the same IF where they receive an appropriate amplitude and phase weighting before being combined to form a separate beam for each multiple access user. In the selection of the components and frequency plan for implementing the multiplexer, the requirements relative to the operation of AGIPA and the data capacity of the multiple access users interact. To determine the appropriate filters to use for multiplexing the channel signals several factors must be considered:

- 1) The individual channel filters must be sufficiently wide to permit passage of the PN modulated data signal without undue degradation due to finite bandwidth and interference symbol.
- 2) The filters must be sufficiently close to ideal bandpass filters so that degradation due to linear distortion is minimized.

*Thirty-two channels are being constructed with two of the thirty-two as spares.

- 3) Interchannel interference (crosstalk) will increase as the channel filter bandwidths are increased. Extraneous crosstalk will cause erroneous signals to drive the adaptive algorithm and will generally slow convergence to the optimum pattern. If the crosstalk is sufficiently large, convergence of the AGIPA algorithm will be prevented. Another effect of crosstalk is that it essentially combines signals from several array elements (i. e., those on adjacent multiplexed channels). This combining effect tends to cause an antenna beam narrowing effect and therefore increases the scan loss of the adaptive array.

The first two factors favor choice of filters having as large a bandwidth as possible. The third factor favors a choice of filters having as small a bandwidth as possible. The problem of filter selection, therefore, entails a tradeoff between various types of system degradation (distortion vs. crosstalk and noise) as well as weight, size and cost of the filters. A further overall constraint is placed on the available bandwidth for the multiplexed signals, resulting in a 6 MHz channel spacing.

The basic approach is to meet the channel requirements, vis-a-vis, bandwidth, phase linearity, amplitude linearity and center frequency with a single IF filter in each array channel. The filter will be at the same frequency in each channel, thereby imparting identical (within filter tolerances) amplitude and phase characteristics to each channel.

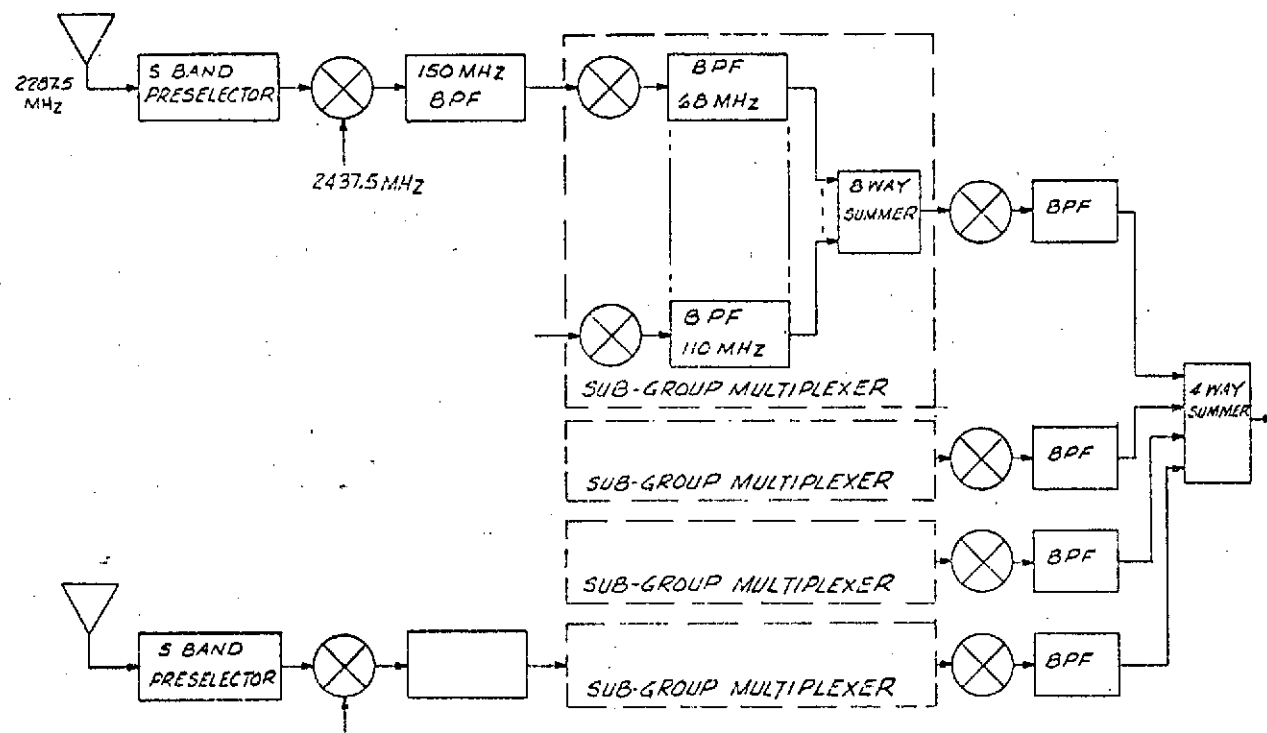
Since the IF filter bandwidth cannot be selected without some consideration of the Mux/Demux system requirements, we will turn now to that subject and reconsider the IF bandwidth and other filter parameters later.

The multiplexer unit must accept 32 channels, combine them in a FDM manner, and upconvert the aggregate signal which is to be transmitted at K_u -band within a 192 MHz bandwidth.* Because of the large number of channels and their spectrum occupancy, it is not possible to individually upconvert and filter each channel equally in a single step. That is, a filter designed with the proper 3 dB bandwidth to yield an acceptable linear phase bandwidth for the lowest center frequency channel would, when translated to a higher frequency channel generally not be acceptable due to an inherent shrinkage of the filter's linear phase bandwidth. To minimize these effects it is recommended that the 32 channels be divided into four groups. There would be eight channels assigned to each subgroup as shown in Figure 2-11. Each group would occupy the identical bandwidth of 54 MHz. By reducing the bandwidth across which the filters have to track (i. e., 48 MHz vs. 192 MHz) we have eased the filter phase bandwidth requirements. Each of the four groups is subsequently upconverted at 48 MHz spacings to a supergroup frequency band whose image is easily rejected. This aggregate signal which is a supergroup occupying the band 272-463 MHz, may in turn be upconverted to K_u -band and transmitted.

The selection of frequencies for performing the down and up-conversion in the multiplexer is also based upon utilizing the existing AGIPA hardware to the greatest extent possible. In this manner the cost of the simulation is minimized. Since the S-band module had originally been designed for an IF output frequency of 135 to 235 MHz, a center frequency of 150 MHz has been selected. The 1st IF frequency must be either above or below the subgroup frequencies to prevent signal feedthrough into the subgroup channels. Therefore a low 1st IF such as 70 MHz would require an initial subgroup frequency of approximately 150 MHz to eliminate 2nd harmonics of the 1st IF from leaking into the 2nd IF. Additionally, a new 1st IF moves the S-band image frequency band that much closer to the desired frequency, incurring an increased loss at the desired signal frequency. Therefore, the selection of a 150 MHz 1st IF eases the image rejection requirements, utilizes

*An allocation of 240 MHz is being reserved for expansion to forty channels.

FIGURE 2-11
MULTIPLEXING APPROACH



the existing hardware and represents both the upper limit for the application of lumped constant filter design and the lower limit for a cavity resonator in terms of size. Therefore, the 150 MHz frequency represents an acceptable tradeoff point where a relatively inexpensive, easily reproducible cavity filter can be employed in the simulation and a lightweight smaller sized filter using lumped components can be developed for the actual flight model of the array.

2.4.2 CHANNEL ISOLATION AND FILTER SELECTION

CHANNEL ISOLATION OF MORE THAN 40 DB IS SELECTED AS A DESIGN GOAL TO BE ACHIEVED WITH A 6 POLE CAVITY FILTER PERMITTING CHIP RATES UP TO 2.5 MB/S.

Channel isolation or the coupling of unwanted energy from one array channel into another occurs either due to the mutual coupling between antenna elements or the mux-demux circuits. Since there will be mutual coupling between elements, any signal induced current in one element will generate a low level current in an adjacent element (see Figure 2-12). This effect has been measured as a function of element spacing, with a variation of 40 to 50 dB for element spacings of 0.5λ to 2.5λ . The measurement neglects other system effects such as pattern distortion or element beam tilting caused by the close proximity of an adjacent element. The ultimate effect of antenna mutual coupling will be a loss of array gain which is basically the reason for using a large element separation.

The second means for energy to leak from one channel into an adjacent channel is through the electronics of the array and more specifically in the multiplexing and demultiplexing operation of the system (see Figure 2-13). Coupling at the antenna will produce a different effect than coupling in the electronics since the signal into an adjacent channel is basically at the same carrier frequency.

As shown in the vector diagram, Figure 2-14A, the coupled energy of other antenna elements will cause the desired vector to rotate to an erroneous phase position and take on a new amplitude. The resultant vector will vary as a function of received signal direction and generally causes a reduction in array gain. Since the coupling level is a function of array element spacing and design, the magnitude of the coupled signals and net effect on system performance can only be roughly estimated with two breadboard elements. The results of the initial tests will be applied to the selection of an array layout which in turn will yield the answer for the thirty element array.

ANTENNA COUPLING

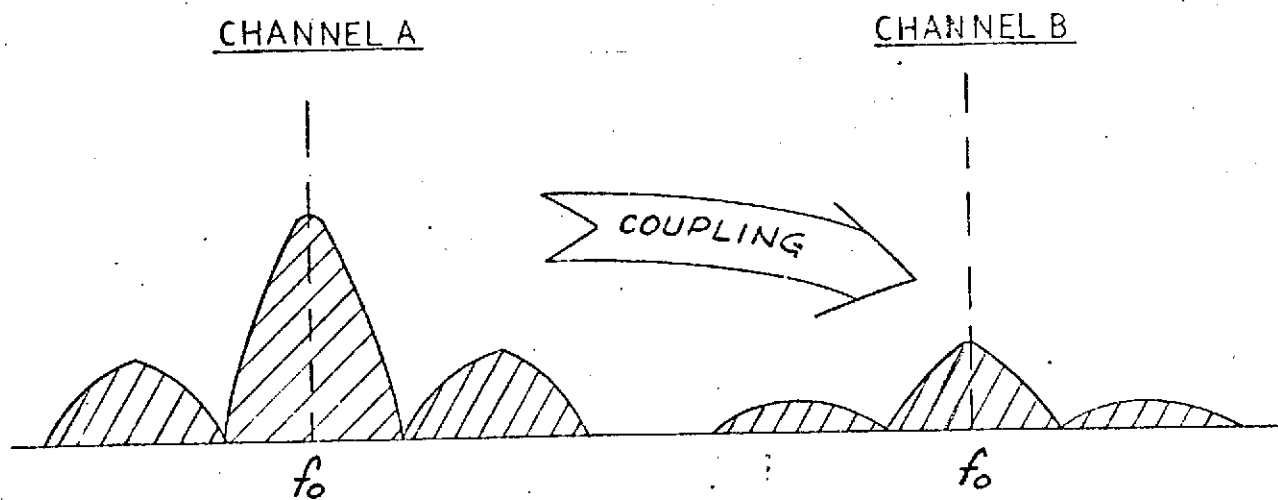


FIGURE 2-12
ANTENNA COUPLING

MULTIPLEXER COUPLING

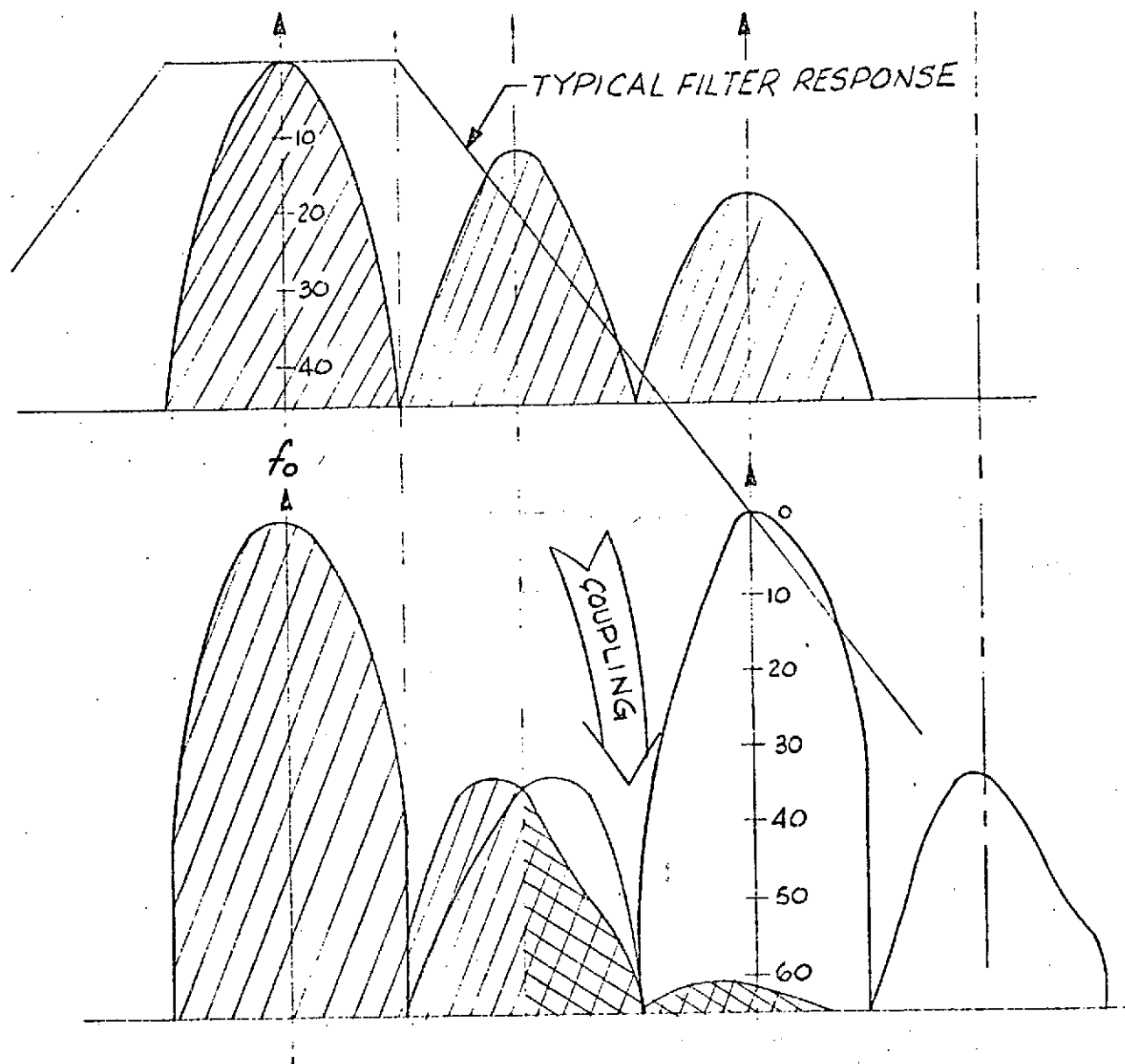
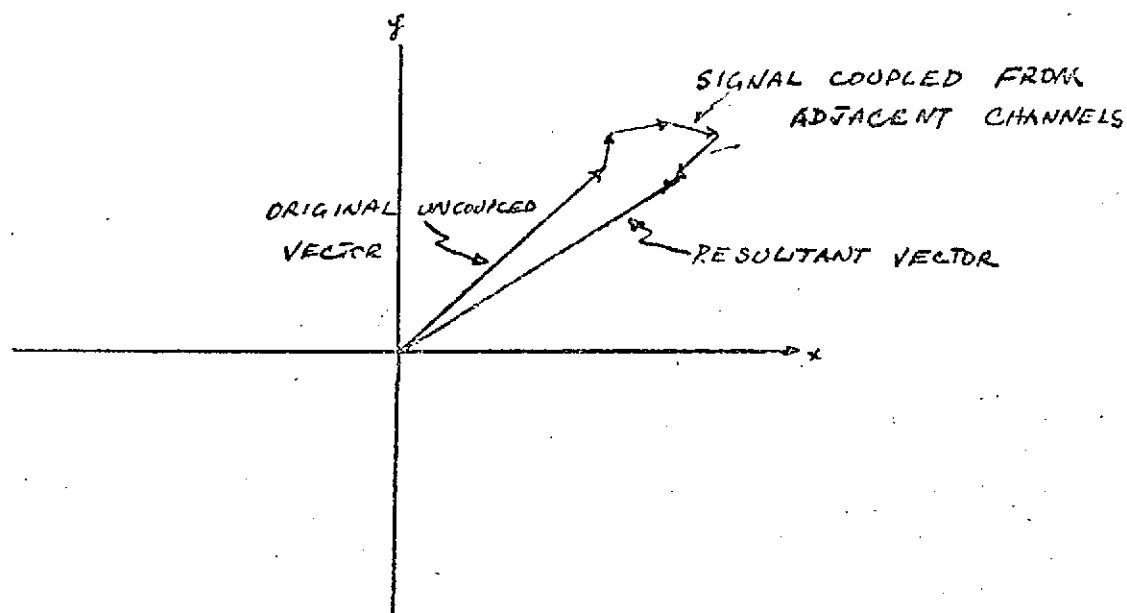
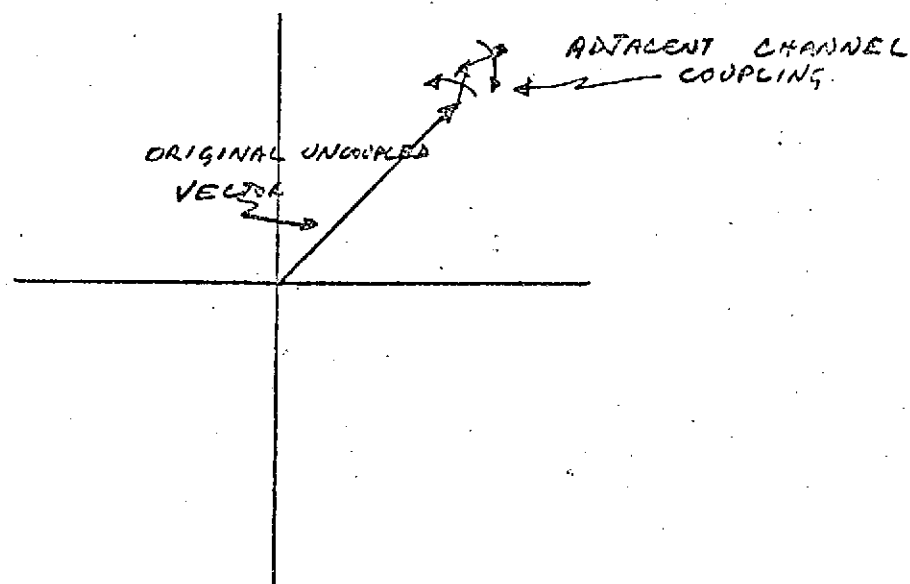


FIGURE 2-13
MULTIPLEXER COUPLING

Coupling in the mux-demux function occurs by means of an overlap of the tails of the adjacent channels rather than in a linear fashion as shown in Figure 2-13.



(A) - ANTENNA COUPLING -



(B) - MULTIPLEXER - DEMULTIPLEXER COUPLING

FIGURE 2-14
VECTOR DIAGRAM OF COUPLED SIGNALS

Since the signal consists of a carrier modulated by a PSK waveform the resulting spectrum is a $\frac{\sin x}{x}$ -function whose energy distribution is dependent upon the PN chip rate selected for the system. The sidelobes of the function are assumed to be received at full strength since selective filtering of the user's saturated transmitter output to limit sideband power would represent a severe weight and power penalty. Filtering before the transmitter will not reduce the sidebands since the limiting action of the saturated amplifier will result in the reinsertion of the original sidelobe levels.

The diagram in Figure 2-14B illustrates the multiplexing filter reducing the sidelobes which spread into an adjacent channel and add at frequencies other than the carrier frequency to the desired channel frequency. The effect on the desired signal, which receives energy from two adjacent channels is to cause a rotation of the original vector similar to noise. (See Figure 2-14B)

Front end noise will also be coupled into the adjacent channels and this also will increase the noise figure or system threshold somewhat.

To select a filter which provides sufficient attenuation of the co-channel interfering signals, the interference levels will be calculated as a function of the filter characteristics. This will be performed independent of the filter phase characteristics, since it will be shown later that for the filters considered a minimum of distortion will result.

Estimation of the signal-to-interference level (S/I) due to crosstalk has been performed utilizing several simplifications which expedite the analysis without causing significant error. To evaluate the channel signal level the desired signal density is assumed to be contained within the required 3 dB bandwidth of a channel for a given chip rate. It has been shown by studies *

* Magnavox Final Report, "Multipath Modulation Study for TDRS" Contract No. NAS-5-10774 for NASA/GSFC, January 1970

and experimental measurements show that a 3 dB bandwidth of 1.5 times the chip rate will result in an overall degradation of less than 1 dB in the received signal. This results from the fact that more than 90% of the signal energy is contained within the 3 dB bandwidth and using the 1.5 criterion, the signal density for a one watt signal is then

$$S(\omega) = 10 \log \left[(1)(1.5)(CR) \right] \text{ dBW} - \text{Hz}$$

where,

$$CR = \text{pseudo-random chip rate} - \text{b/s}$$

The sidelobe or co-channel interference level is estimated by calculating the peak level of the first sidelobe which appears in the adjacent channel. This energy is assumed to be uniformly spread over the 6 MHz bandwidth of the adjacent channel as shown in Figure 2-15 for the four chip rates considered (1.5 Mb/s, 2.0 Mb/s, 3.5 Mb/s, 3.0 Mb/s).

The unattenuated interference level is then

$$I(\omega) = 10 \log (1)(.04)(6 \times 10^6) = 53.8 \text{ dBW-Hz}$$

For filters implemented with 4, 5, and 6 poles, the attenuation is that obtained at the channel crossover point shown in Figure 2-15. The entire $I(\omega)$ term is then assumed to be rejected by an amount equivalent to the attenuation occurring at the crossover point. By neglecting the effect of the continued filter roll-off, the results presented in Table 2-5 are slightly pessimistic but this will account for noise from several channels away as well as second order leakage effects through the local oscillator lines. As shown in Table 2-5, the S/I varies from a high of 69.7 dB for the six pole narrow bandwidth case to a low of 23 dB for the wideband case.

* AIL final report, AGIPA, NAS-5-21653, February 1973

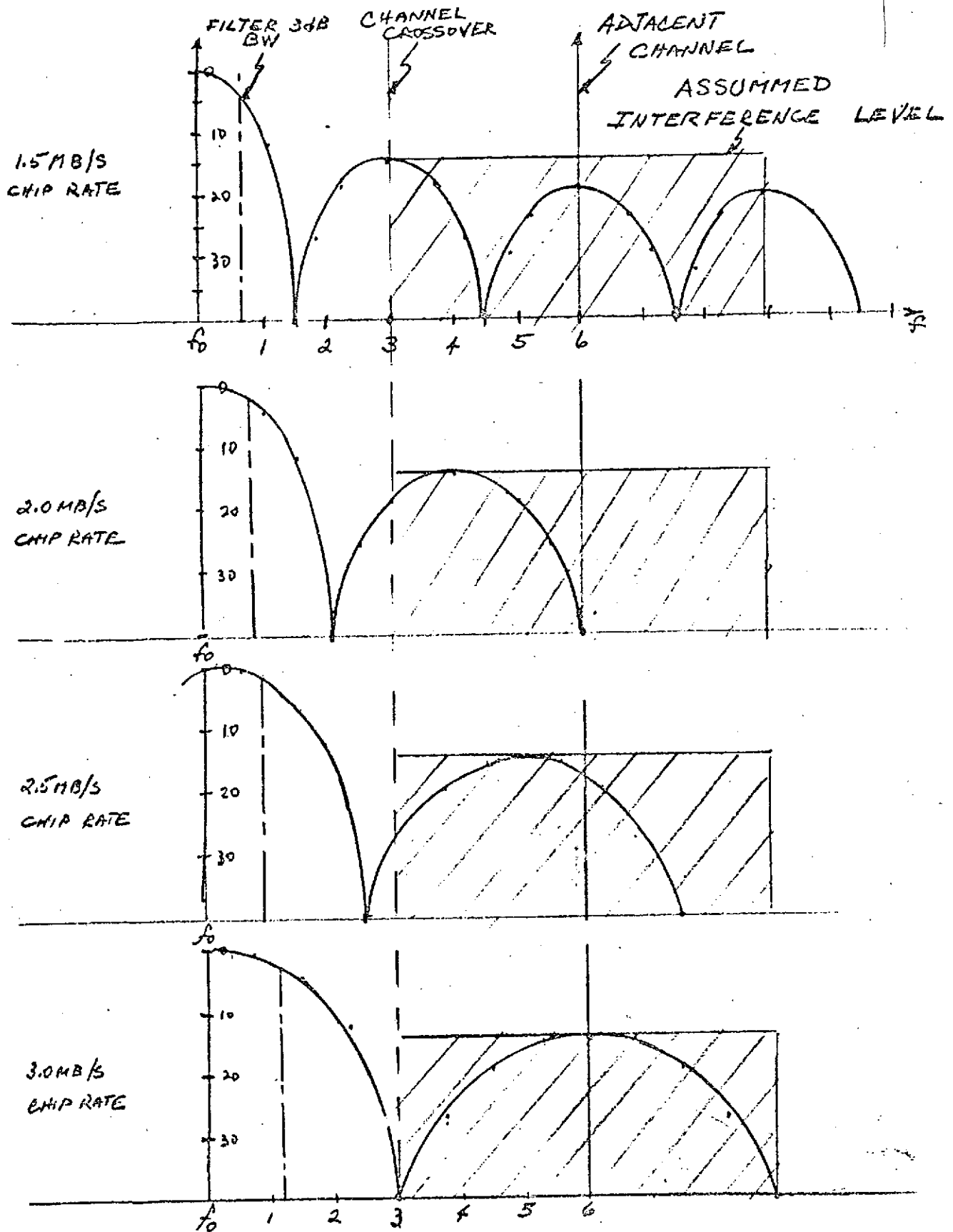


FIGURE 2-15

TABLE 2-5
FILTER TRADEOFF

Chip Rate MB/s-3 dB BW	Signal Density S(w)-dBw-Hz	Interference I(w)-dB-Hz	Attenuated Interference-dBw-Hz			Signal-to- Interference dB		
			4 Pole	5 Pole	6 Pole	4 Pole	5 Pole	6 Pole
1.5-2.25 MHz	63.5	53.8	21.8	9.8	-6.2	41.7	53.7	69.7
2.0-3.0 MHz	64.8	53.8	33.8	23.8	8.8	31	41	56
2.5-3.75 MHz	65.7	53.8	38.8	33.8	23.8	26.9	31.9	41.9
3.0-4.5 MHz	66.5	53.8	43.8	38.8	33.8	23	27.7	32.7

The filter implementation used to compile the information in Table 2-5 is a cavity filter which can achieve relatively high Q's in a reasonable size. These filters are available with rapid delivery and can provide the desired phase tracking and linearity requirements.

Before selection of a filter several additional considerations are required. These include phase linearity and amplitude ripple requirements of the filter. Because the Chebyshev filter has a smaller noise bandwidth vs. 3 dB bandwidth for odd filter order greater than two, it is widely employed for communication link purposes. For the same reason, a Chebyshev response is desirable in the multiplexer. The system performance with this type of filter is dependent not only upon the selection of its bandwidth and the number of its poles, but also on the amount of ripple experienced in the passband. Filter degradation for PSK signals is, however, independent of passband ripple up to approximately 0.1 dB ripple*. Between 0.1 dB and 1.0 dB ripple, degradation rises gradually, however, above 1.0 dB it increases rapidly. To ensure that there is minimum degradation to the channels prior to multiplexing, the passband ripple will be selected as 0.05 dB, well within the stated degradation margin.

* J. Jay Jones, "Filter Distortion and Intersymbol Interference Effects on PSK Signals", IEEE Trans. Comm. Tech., Vol. COM-19, April 1971. pp. 120-132

In addition to the degradation due to the amplitude of the channel frequency response, there will also be degradation due to a non-linear phase vs. frequency characteristic. It has been shown that the effective * degradation due to this effect on a PSK-PN spread spectrum is

$$L = -20 \log_{10} \langle \cos \phi(f) \rangle \text{ dB}$$

where $\phi(f)$ represents departure from a linear phase characteristic and $\langle \cdot \rangle$ denotes an average weighted by the spectral power density across the passband. Removal of the weighted average and using ϕ as a maximum deviation from a linear phase response leads to a pessimistic assumption and the conclusion that a $\pm 20^\circ$ tolerance corresponds to a degradation of less than $-.54 \text{ dB}$. We see, therefore, that performance is relatively insensitive to phase response non-linearity. Since a $\pm 10^\circ$ tolerance on phase response non-linearity is not an unduly severe filter requirement, this will be taken as a nominal filter requirement for individual channel filters.

2.4.3

ARRAY PERFORMANCE EFFECTS

To this point, with the exception of channel isolation, the performance of the array has not been considered in the filter selection. The processing circuits must transfer the signals to the ground so that the thirty element sum can produce a signal which is thirty times larger with respect to noise. The effect of channel amplitude ripple, phase non-linearity, phase differences across the frequency band between channels will ultimately effect the summation. The most straight forward method to achieve phase tracking between channels is to identically implement the network which determines the phase response. Therefore, even though each channel is eventually translated to a different frequency band, the 150 MHz filters tend to desensitize the channel to further phase deviations and, thus, de-emphasize their effects.**

* LeFande, R.A., "Effects of Phase Non-Linearities on Phase-Shift-Keyed Pseudo-noise/Spread Spectrum Communications", IEEE Trans. on Comm. Tech., October 1970, Vol. Comm.-18, pp. 685

** Op Cit Jones

Therefore, by selecting filter bandwidths for all other filters in the system to have greater than a 6 MHz 3 dB bandwidth with a phase linearity over this band of better than $\pm 5^\circ$, we can be assured that the 150 MHz filter will produce the major effect. Appendix II presents an analysis of the phase errors by considering that at any one frequency across the band, the addition of N array signals will produce a desired term and a randomly distributed term which is representative of the lack of uniformity between channels. An expression for the signal-to-phase noise term is derived and the result is:

$$\rho = \frac{3N}{\epsilon^2}$$

where:

ρ = signal-to-phase noise

N = number of elements in the array

ϵ = phase error in radians

The expression is plotted in Figure 2-16 for thirty and forty element arrays. To achieve a ρ greater than 40 dB, the phase tracking errors between channels should be less than $\pm 5^\circ$. This specification represents the limit of what can be practically achieved in identical filters over a temperature range of $+10^\circ\text{C}$ to $+40^\circ\text{C}$. Therefore, a specification of $\pm 5^\circ$ is selected for the IF filter. This will result in a somewhat larger phase error figure after all the channel components are included.

2.4.4

ADAPTIVE PERFORMANCE

A series of computer simulation tests were run on the AGIPA system to evaluate the effect of crosstalk on the performance of the adaptive system. The crosstalk simulated was of the type experienced by antenna mutual coupling due to the limitations of the computer program. Initial tests were run against the previously specified jamming scenario and for crosstalk levels of from -30 dB to -5 dB, insignificant differences were noted in nulling ability or

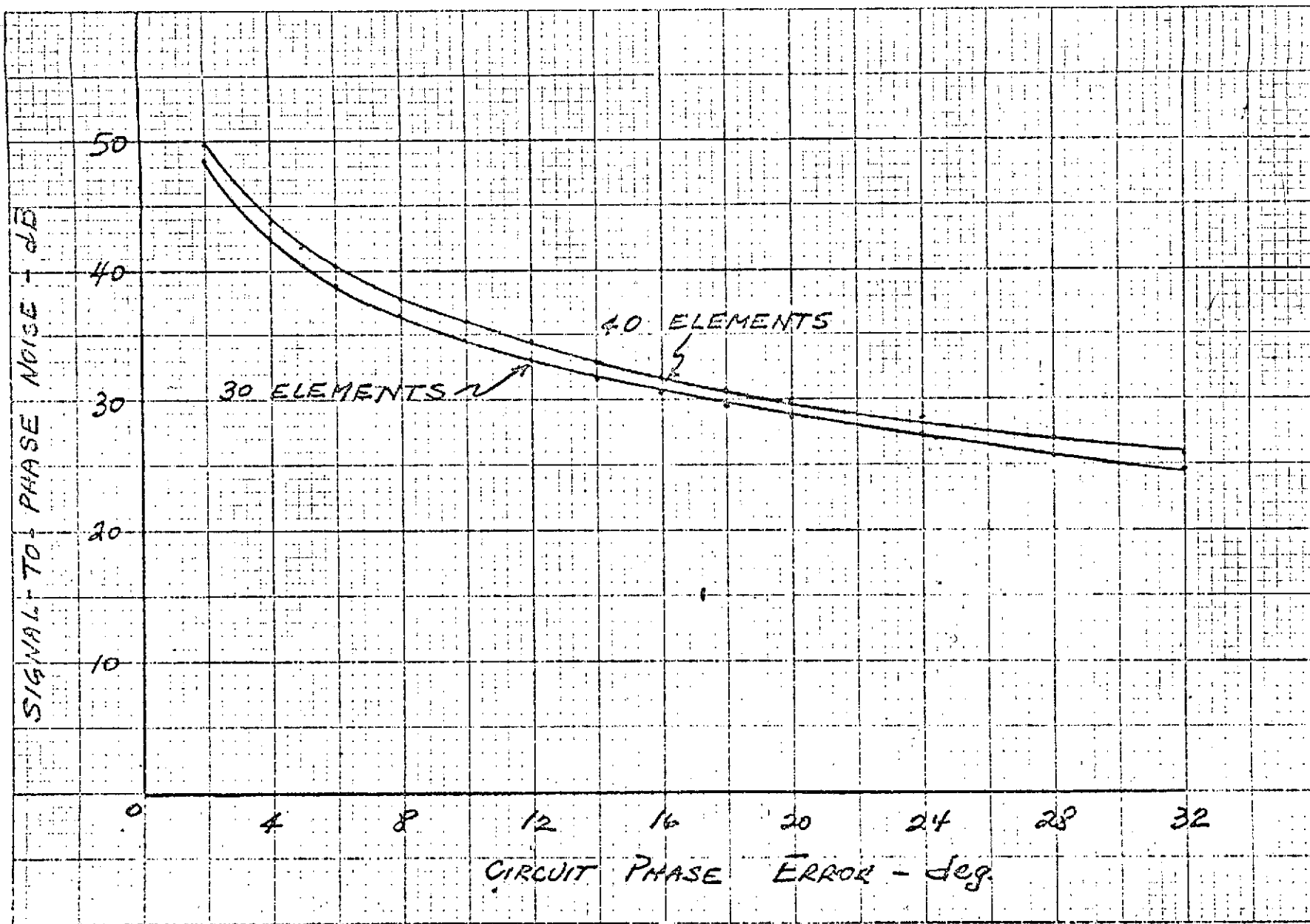


FIGURE 2-16

SIGNAL-TO-PHASE NOISE vs. CIRCUIT PHASE ERROR

the number of steps required of the algorithm to achieve a null. Because of the large number of elements, the effect of sub-arraying small groups of the thirty elements are not seen, as the adaptive process can still null the relatively small number of jammers. The only performance difference noted occurred in an increased scan loss for the simulated system. Similar tests made with a five element array, where the number of jammers exceeds the degrees of freedom the array offers in forming nulls, indicated more significant performance degradation. The five element array had large increase in convergence time for a crosstalk level of -10 dB.

These tests, although providing some additional insight into array performance with crosstalk, are inconclusive and the final system performance tests will have to be conducted before a conclusion can be reached on crosstalk.

For interference generated by the filtering process, the effect on array performance will impact the system at the point where the summed array signal is correlated with the individual element signals to generate the steering signals for the element weighting networks. Since adjacent channel signals will be present in the channel being compared with the sum, this coherent interference will generate erroneous voltages out of the correlator. Since the correlator output is read into the computer with an eight bit A/D converter, with a voltage resolution of 256 bits $\pm 1/2$ bit, the crosstalk would have to be greater than 48 dB below the desired signal to change the correlator by one bit. Since the correlator voltages are measured in a 100 Hz bandwidth, the thermal noise level is 20 dB below signal for 1 Kb/s users and 40 dB below signal for 100 Kb/s users (assuming a received $C/N_0 = 9.9$ dB for $P_e = 10^{-5}$). Therefore, if the crosstalk is below the noise level or 40 dB below the signal, its effect should be negligible. Referring back to Table 2-5, this S/I ratio can be achieved for several chip rates with standard filters.

2.4.5

FILTER SELECTION SUMMARY

The filter specifications are developed considering crosstalk, distortion, phase tracking, system requirements, and filter size. As previously developed, a minimum crosstalk level of greater than 40 dB is desirable to keep the crosstalk below noise. The system requires a maximum chip rate so that the multiple access users are separated by the largest possible code isolation. Therefore, a bandwidth of 3.75 MHz is selected to achieve a reasonable size filter, maximum channel bandwidth, and a high probability of the array performance not being degraded by crosstalk. The filter data is summarized in Table 2-6.

TABLE 2-6

FILTER SPECIFICATION

Center Frequency	150 MHz
Bandwidth - 3 dB	3.75 MHz
Bandwidth - 30 dB	6 MHz
Bandwidth - 60 dB	12 MHz
Phase Linearity over ± 1.5 MHz	± 10 deg.
Phase Tracking over ± 1.5 MHz	± 5 deg.
Amplitude Ripple	0.15 dB
Number of Poles (cavity)	6
Loss	4.5 dB

2.5 CODE ISOLATION AND ALTERNATE OPERATING MODES

PRELIMINARY CONSIDERATIONS WHICH REQUIRE EXPERIMENTAL OR ANALYTICAL VERIFICATION INDICATE THAT THE AGIPA SYSTEM CAN FUNCTION WITH THE CHIP TO BIT RATIO PROVIDED BY CHIP RATES FROM 1.5 Mbps TO 3.0 Mbps. SEVERAL ALTERNATIVE OPERATIONAL MODES ARE RECOMMENDED FOR AGIPA, NAMELY, THE ADAPTIVE MODE WITH AND WITHOUT A PILOT, THE OMNISCIENT MODE, THE CONTRIVED SOLUTION MODE AND THE DATA AIDED LOOP MODE. FIXED OPERATION LIMITING FLEXIBILITY IS NOT THE RECOMMENDED APPROACH.

In forming custom beams for each individual user the AGIPA processing circuits depend to some extent on the code isolation properties afforded the multiple access users. The basic AGIPA processing circuits compute a change in the required weights for an individual array channel using the relationship

$$\Delta W = \left[\begin{array}{l} \text{SIGNAL} \\ \text{CORRELATIONS} \end{array} - \begin{array}{l} \text{OTHER USER} \\ \text{INTERFERENCE} \\ \text{CORRELATION} \end{array} \right]$$

where ΔW is the change in channel weights.

Basically, the desired signal waveform is compressed to the data bandwidth by a locally generated reference code, while the interference due to other users is spread over the IF bandwidth. The system implementation then employs a bandpass filter to select the signal waveform and a band reject filter (the signal energy is rejected) to measure the interference correlations. Both correlations provide analytic signals comparing the summed array output with the signal and interference present on an individual channel.

Current specifications on the TDRS link call for use of a 2047 chip ($2^n - 1 = 2047$, $n = 11$) Gold code carrier signal to provide spread spectrum multiple access capability for up to 20 simultaneous users. A chip rate (CR) of 1.5 Mb/s is contemplated.

Based on correlation properties of Gold sequences as described in * an $n = 11$ Gold code sequence could provide a minimum user-user isolation of

$$20 \log_{10} \frac{2^n - 1}{2^{(n+1)/2} + 1} \approx 30 \text{ dB}$$

To provide this isolation, a correlation period of at least 2047 chips is required.

Consider the minimum data rate of 1 Kb/s and a Gold code length of 2047 chips. To achieve the ideal isolation at least 2047 chips must be contained in a data bit. The minimum chip rate will therefore be 2.047 Mbs. Chip rates smaller than this will cause degradation in multiple access performance since less than ideal user isolation will result. The result of the reduced isolation between multiple access users with respect to AGIPA is that a portion of the interference energy appears as correlated signal. Therefore, in the above expression, a larger portion of the interference energy will appear in the signal channel than predicted. The signal correlation, containing small amounts of interference, will cause the convergence time of the algorithm to increase since the computer measure of performance will rely more heavily on the interference channel. Therefore, some degradation in performance can be expected and it will most probably appear as an increase in the convergence time of the algorithm and the depth of the nulls formed.

To evaluate the magnitude of the problem let us initially assume that a CR of greater than 2.047 Mb/s exists in the system and that the code isolation is 30 dB for each interference. For receiving data at a rate of 1 Kb/s the interference which will be present in the 1 Kb/s signal channel after despreading is approximately (neglects multipath)

$$I = \frac{P + 2P(10) + 3P(30) + 2P(100)}{1000}$$

where P is the signal power in the 1 Kb/s channel and the interference scenario is the same as shown in Figure 2-7

*R. Gold, "Optional Binary Sequences for Spread Spectrum Multiplexing" IEEE Trans. on Info. Theory, October 1967

$$I = 0.311P$$

$$P/I = 5.0 \text{ dB} = \text{resultant code rejection}$$

To this amount of code rejection the minimum beam rejection of the pointed array is added. The beam rejection was computed for Figure 2-8 and using the worst case rejection which occurred at position #2, the rejection is 12.43 dB. This rejection is determined by calculating the S/I ratio of a FOV element which received the radiated interfering and signal power equally. To the beam rejection is added 5.1 dB code rejection from above resulting in approximately 17.5 dB of interference rejection. Therefore, for the 1 Kb/s a S/I above threshold is available.

For the 100 Kb/s user, the code isolation would be significantly less than the 1 Kb/s since integration over less than a full code period would be used. To evaluate the isolation properties of Gold codes for the situation where the integration window, W , is less than the variance of the partial correlation function of two codes has been derived as*

$$\sigma^2 = w \left[1 + \frac{w-1}{2^{2n-1}} \right] \approx w$$

The standard deviation for this function is,

$$= \sqrt{w}$$

and including all cases between 2 times the standard deviation, the isolation for partial codes is approximated using the example of Gold's previous expression by

$$ISOL = 20 \log \frac{w}{2\sqrt{w}} = 10 \log \frac{w}{2}$$

Table 2-7 lists the reduction in multiple access isolation for the chip rates under consideration. The first entry of the Table lists the S/I ratio which would exist for the selected user scenario by summation of all other user powers compared to relative power at the data rate in question. For each data rate the code isolation is estimated and the resultant S/I ratio is computed for code isolation alone, the addition of a fixed 7 dB

*Magnavox, "Multipath/Modulation Study for the TDRS System", Contract No. NAS-5-10744, January 1970

improvement due to a pointed beam and finally with an additional improvement of 3 dB for the 100 Kb/s user and 10 dB for the others due to AGIPA. From this tabulation it can be seen that a system which employed a pointed beam for code acquisition and then switched to adaptive processing would have sufficient margin to successfully operate in all but the 30 Kb/s mode. Should the PN code acquisition loop prove to have difficulty acquiring in the pointed beam mode or should the AGIPA processing circuits fail to provide sufficient nulling due to the lack of code isolation, several alternatives exist. These alternatives are:

(1) Coded Pilot

Use of a coded pilot to be transmitted along with the data bearing signal but bearing only the user code. This pilot could be separated at the receiver and since it does not bear any data, can be put through a narrow band filter sufficiently narrow to achieve integration over the full correlation period. This approach makes the user-user isolation independent of data rate. Therefore, even longer codes can be used to improve the multiple access capability without limiting data rate. Of course, additional power would be required to transmit the pilot required in this approach. For the 100 Kb/s case using an integration bandwidth of 100 Hz would require a pilot 30 dB below the data signal power and achieve approximately dB additional code isolation over the results in Table 2-7. For the lowest data rate users the listed code isolation may prove to be sufficient but the 30 Kb/s and 10 Kb/s users may require additional protection. This can be verified during the test program.

(2) Omniscient Solution

Since the position of each user, its transmitted power and data rate are known at the ground station, the possibility of utilizing this data to compute the optimum weight settings directly (this involves a matrix inversion) without measurement of desired signals and interference for adaptively reaching the optimum settings. Working in favor of this approach is the slowly changing user

TABLE 2-7
CALCULATED PERFORMANCE OF MULTIPLE ACCESS SYSTEM

DATA RATE	INITIAL S/I-dB	CHIP RATE (Mb/s)	CHIPS/BIT W	EST. CODE ISOLATION	CODE REJ.	S/I RATIO WITH BEAM REJECTION (dB)	WITH AGIPA
100 KB/S -3.2		1.5	15	8.75	5.55	12.55	15.557
		2.0	20	10.0	6.8	13.8	16.8
		2.5	25	11.0	7.8	14.8	17.8
		3.0	30	11.8	8.6	15.6	18. 3 dB improvement
30 KB/S -9.7		1.5	50	14.0	4.3	11.3	21.3
		2.0	67	15.2	5.5	12.5	22.5
		2.5	83	16.1	6.4	13.4	23.4
		3.0	100	16.9	7.2	14.2	24.2
10 KB/S -14.8		1.5	150	18.8	4.0	11.0	21.0
		2.0	200	20.0	5.2	12.2	22.2
		2.5	250	20.9	6.1	14.2	24.2
		3.0	300	21.7	6.9	13.9	23.9 10 dB improvement
1 KB/S -24.9		1.5	1500	29.0	4.1	11.1	21.1
		2.0	2000	30.0	5.1	12.1	22.1
		2.5	2500	30.0	5.1	12.1	22.1
		3.0	3000	30.0	5.1	12.1	22.1

environment. Accuracy and stability of channel phase and amplitude settings (this could be handled by calibration) and the turning on of unexpected interference are the only limitations.

(3) Contrived Solution

In this approach, using the known position of the desired user, only the interference is monitored, while the signal correlations are computed based on radiation from a known point in space ("contrived") and the adaptive process functions to reduce interference. Computer simulation of this approach has been very encouraging and excellent performance has been obtained.*

(4) Data Cancellation Loop

Utilizing a delay line to permit detected data to remove data transitions from degrading the code isolation of signals feeding either AGIPA or the code acquisition circuits, APL** has bread-boarded this technique and promising results have been obtained. The loop does depend on a prior synchronization mode for code acquisition which may be a disadvantage should reacquisition be needed during a message transmission.

In conclusion, the system can be designed to successfully operate in a number of ways and limitations of one mode in a given situation can be compensated for by switching to a secondary operating sequence. The point is that the system design need not and should not be limited to a single rigid operational philosophy.

* J.M. Smith, A. Zeitlin "Beam Optimized Multiple Access",
Unpublished paper,

** Conversation with F. McIntyre, APL

3.0 DETAIL DESIGN

A DESCRIPTION OF THE ENTIRE TDRS SYSTEM TO BE FABRICATED BY AIL IS DESCRIBED. EACH ASSEMBLY AND SUBASSEMBLY DEFINED. THE SYSTEM DESIGN GUIDELINES AND EXPECTATIONS DEFINED.

A simplified block diagram of the TDRS Simulation System may be seen in Figure 3-1. The simulated TDRS system is made up of three major assemblies. There is, to the left of the figure, that equipment associated with simulating the TDRS environment and labeled appropriately Scenario Equipment. The scenario equipment supplies ten independent S-band sources all at a nominal center frequency of 2287.5 MHz. To simulate closely the expected TDRS environment each S-band interference source is PSK modulated with a different Gold code from the same family of codes as the desired user employs. The clock rate generating the Gold code for each code generator is at a nominal rate of 2.0 MHz. As a part of the scenario equipment AIL will supply, as previously in the AGIPA feasibility program (NASA Contract No. NAS-5-21653), an ICON drive unit which may be employed to vary the position of the track mounted desired user antenna. The satellite equipment assembly in the upper portion of Figure 3.1, employing its S-band converter IF assembly, accents, translates to IF and amplifies the received signals from the ten interfering sources plus the desired user. The satellite then converts in a frequency division multiplex (FDM) manner the translated common IF outputs from the thirty element helix array into a single wideband aggregate signal. The conversion to a single FDM signal is accomplished by the multiplexer assembly in a two part sequential operation. The multiplexer forms first, four eight channel subgroups (i. e., Subgroup I through IV), and then by proper translation in the Supergroup assembly a single signal of four adjacent subgroups is formed.

A forward link which is employed to transmit command data on a single channel to the multiple access users' data received from the ground, has also been made available in the satellite assembly. A phase locked frequency source, which acquires a ground station generated pilot, supplies to the satellite, in a coherent manner, all of the frequencies required for the multiple signal processing operations.

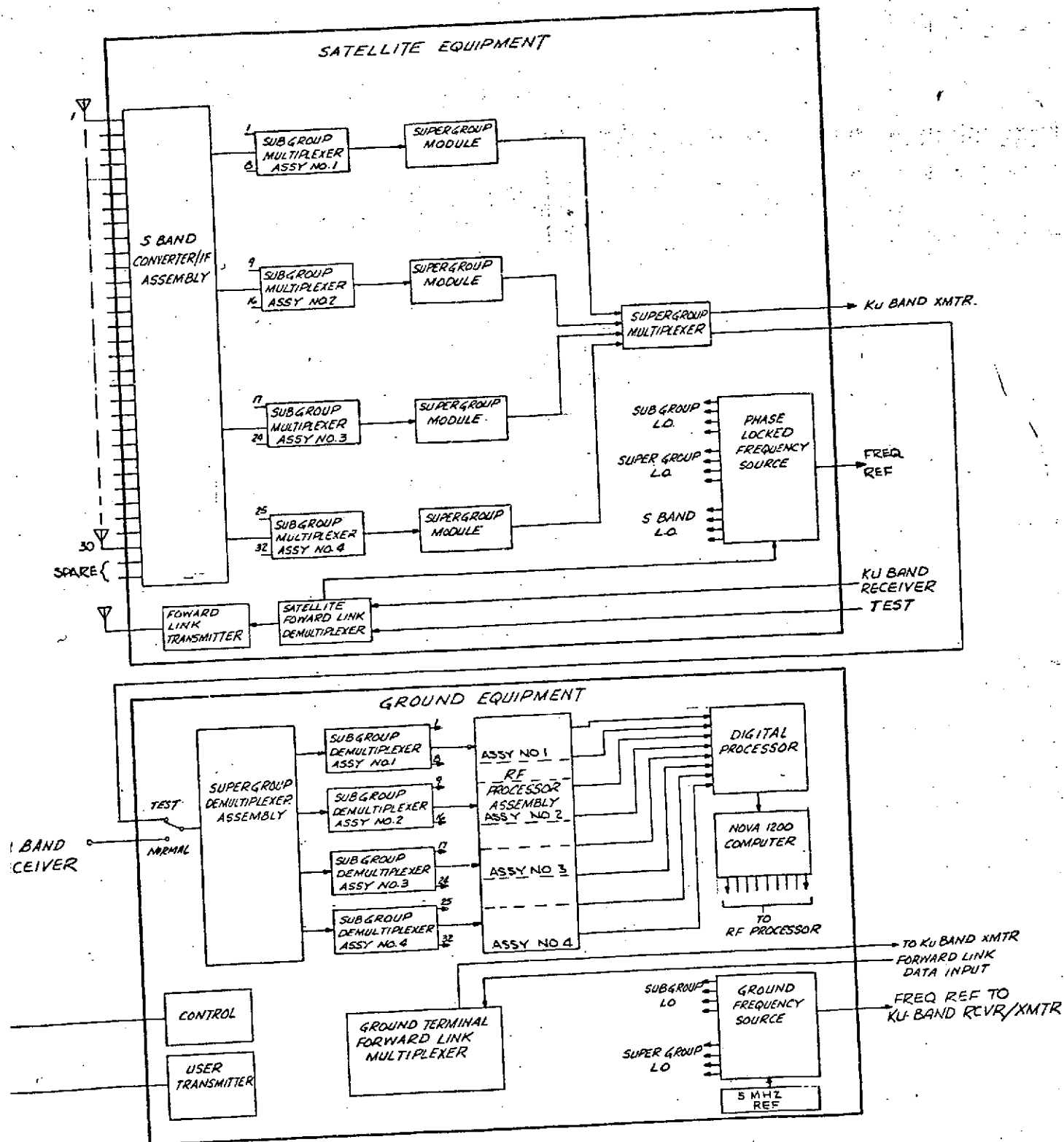
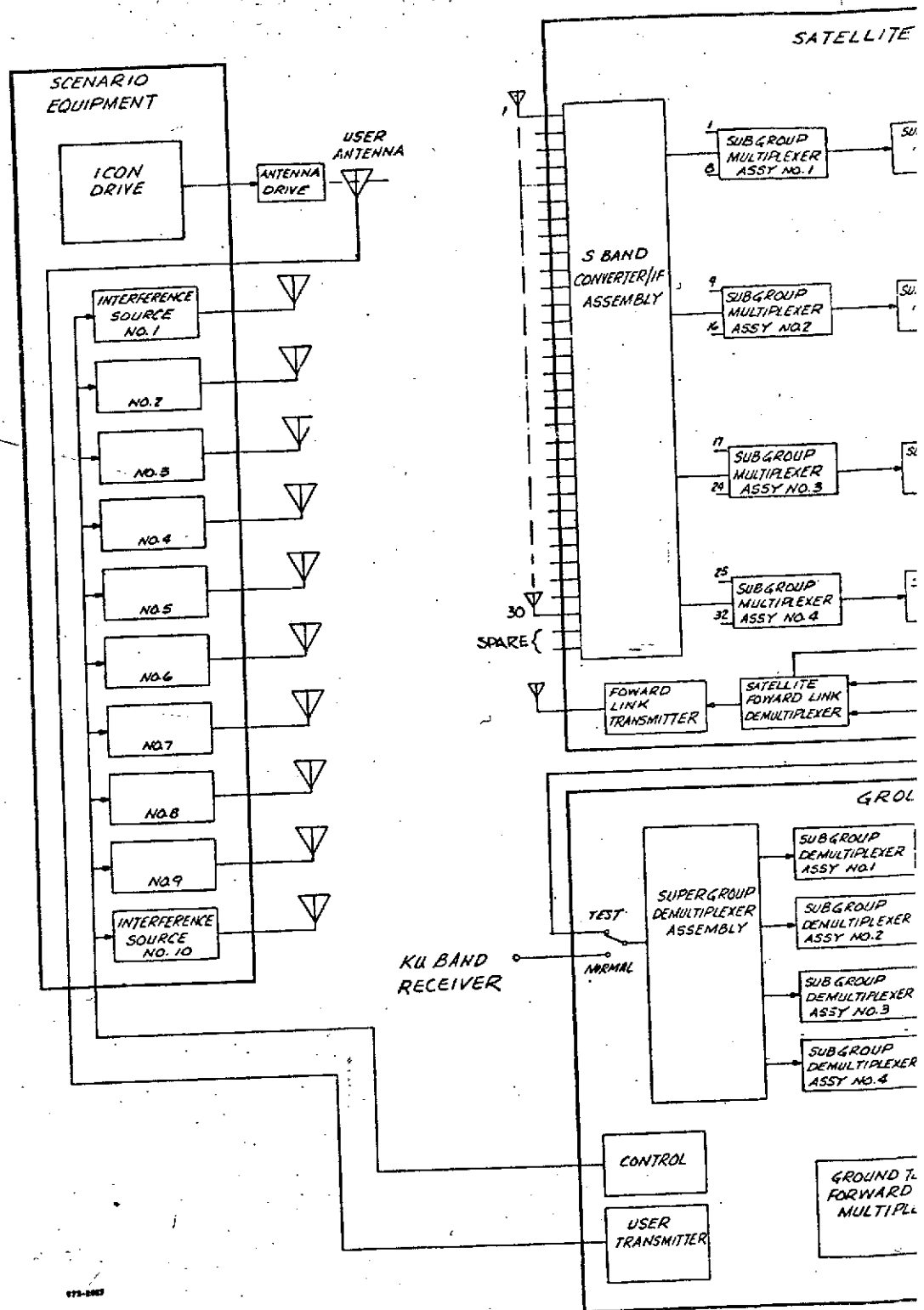


FIGURE 3-1
TDRS SIMULATION SYSTEM



The ground station equipment accepts the single aggregate FDM signal described above either from the K_u -band ground station receiver or directly from the satellite equipment. An RF switch implements the decision between the "normal" mode or "test" mode for the ground station. While the system is at AIL the system will be in the "test" mode thus accepting an inverted FDM spectrum directly from the satellite assembly. The spectrum is inverted in the "test" mode to reflect the inversion which will occur in the signal's passage through the K_u -band S/C to GS link. The ground station, in a two-step operation similar to the one described above for the multiplexer except in inverse order, restores the original 30 channels to a common IF in the Demultiplex assembly. The thirty signals are then fed to the RF processing assembly which in turn supplies two outputs to the Digital Processor. One output is the weighted sum of the thirty channels while the other is an unweighted sample of one of the thirty channels. The weighting of the individual channels and the selection of the sampled channels are under the direction of the system computer.

The system computer "weights" the various channels based on information supplied to it by the digital processor. The digital processor performs cross-correlation measurements between the weighted sum signal and the selected sampled channel. This information in conjunction with power level measurements of the desired signal and interference components is sufficient to drive the algorithm stored in the computer to the proper solution.

The control unit allows for remote control of the amplitude of the ten interfering users found in the scenario assembly. The user transmitter supplies a PSK modulated S-band signal to the scenario assembly which in turn feeds it to a track-mounted linear dipole antenna. The ground station frequency source is the overall system standard and supplies all of the frequencies required by the ground station as well as a pilot signal to the satellite phase locked frequency source.

The system design which will be unfolded in the subsequent sections employs a philosophy of using proven or off-the-shelf hardware, flexibility and commonality. Signal levels throughout the system were raised to levels as high as possible compatible with a design philosophy that calls for intermodulation products at least 60 dB down from the signal level. Each component and the levels expected at that component were

scrutinized for adherence to this rule. Each drawer assembly, and each subassembly and individual unit, in this system employs individual RFI filtering to both protect the unit and to protect other units from it. Most of the assemblies that follow are made up of multiple printed circuit boards. These boards employ a teflon glass dielectric (i. e., FLGT032C1/1) which, although a little more difficult to work with than the fiberglass epoxy material often employed, provides a more stable dielectric constant and thus insures greater repeatability for the multiple units. Each printed circuit board, to insure stability, employs plated through holes to maintain a constant ground on both sides of the board. Each individual unit is housed within its own RFI shielded compartment or enclosure and in turn each assembly is similarly protected.

Wherever possible monitoring RF test points and adjustable gain has been supplied to each module. These features are both convenient to the alignment of the system and allow for future change in conditions required for performance evaluations. To help maintain costs at as low a level as possible, an attempt at commonality wherever possible was implemented. Many of the components such as amplifiers, attenuators, etc. that will be seen in the subsequent sections are used extensively throughout the system and are therefore cataloged in Appendix I. The following sections describe in detail all of the assemblies that make up the TDRS Simulation System.

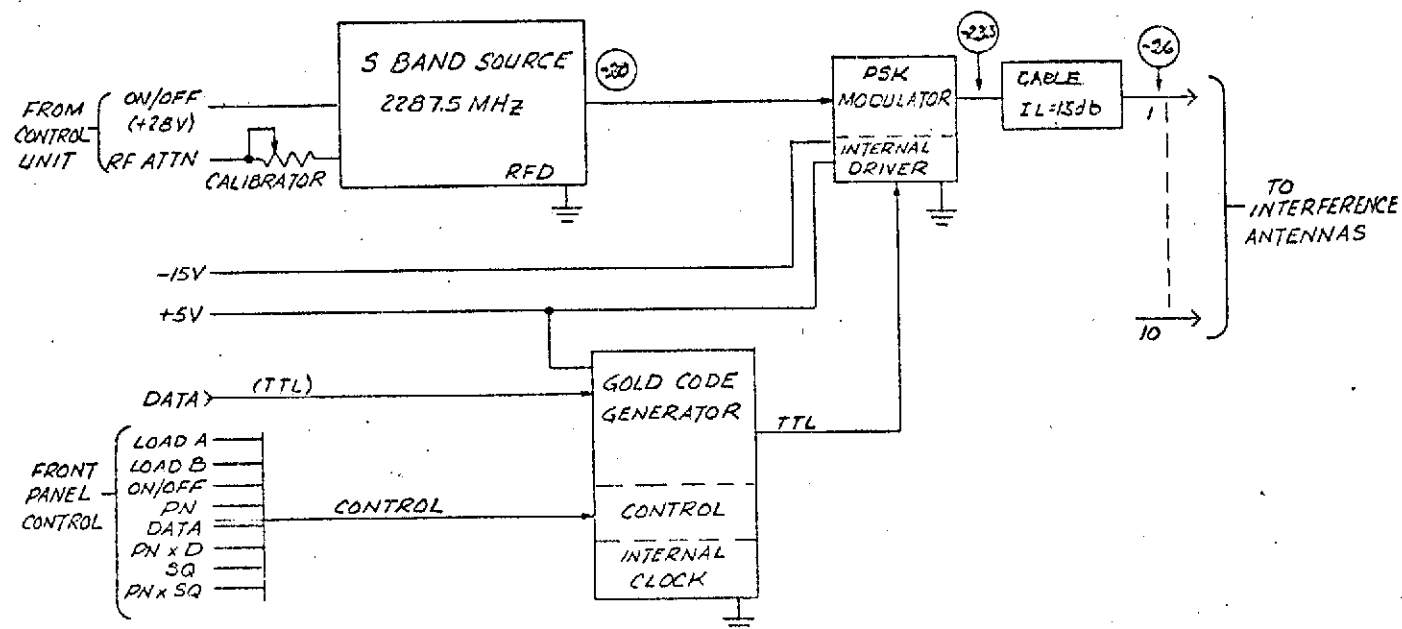
3.1 SCENARIO EQUIPMENT

SIMULATED ELECTROMAGNETIC ENVIRONMENT PROVIDES FOR EFFECTIVE SYSTEM TESTING. BY PROVIDING TEN NONCOHERENT USER FREQUENCY SIGNALS EACH PSK MODULATED WITH A DIFFERENT MEMBER OF THE SAME GOLD CODE FAMILY, A REALISTIC ELECTROMAGNETIC SCENARIO IS AVAILABLE FOR SYSTEM EVALUATION.

The Scenario Assembly is composed of ten simulated RFI sources each representing a potential user of the multiple access system. Each RFI source will be modulated with a different Gold code of the same length, 8191 bits or 2047 bits. The design of the interference sources is such that data, or a square wave at a fraction of the clock rate, may also be added to the PN coding. The output power of each interference source has a variable output range of 50 dB and may be individually turned on or off remotely.

All of the electronics associated with the ten sources are contained within two drawers. Within each drawer there are five interference modules individually enclosed within an RFI shielded compartment. To further insure each module's independence, all control and power lines entering each compartment pass through EMI filters. The sources are composed of the three major units depicted in Figure 3-2. The final S-band output signal is derived from the PSK modulator module which is keyed to the generator logic.

The code generator logic is shown in block diagram form in Figure 3-3. The clock source for each generator can be a single IC shown at the lower left of the diagram. An input control line can disable the clock and thereby set the output to the "no modulation" state. Each clock pulse which arrives at the monostable is narrowed to 150 nanoseconds and drives shift registers A and B.



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FIGURE 3-2
INTERFERENCE SOURCE ASSEMBLY

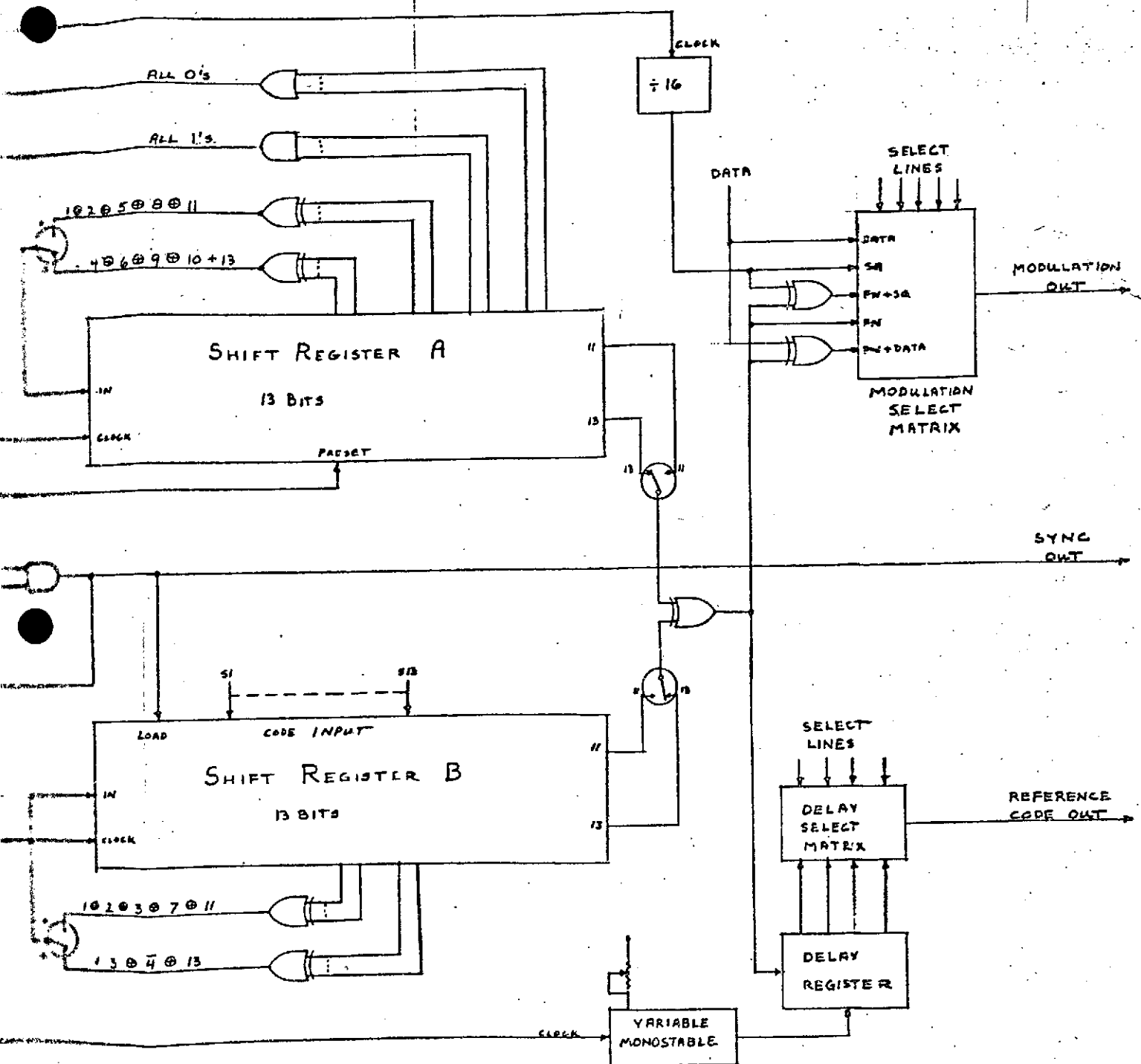
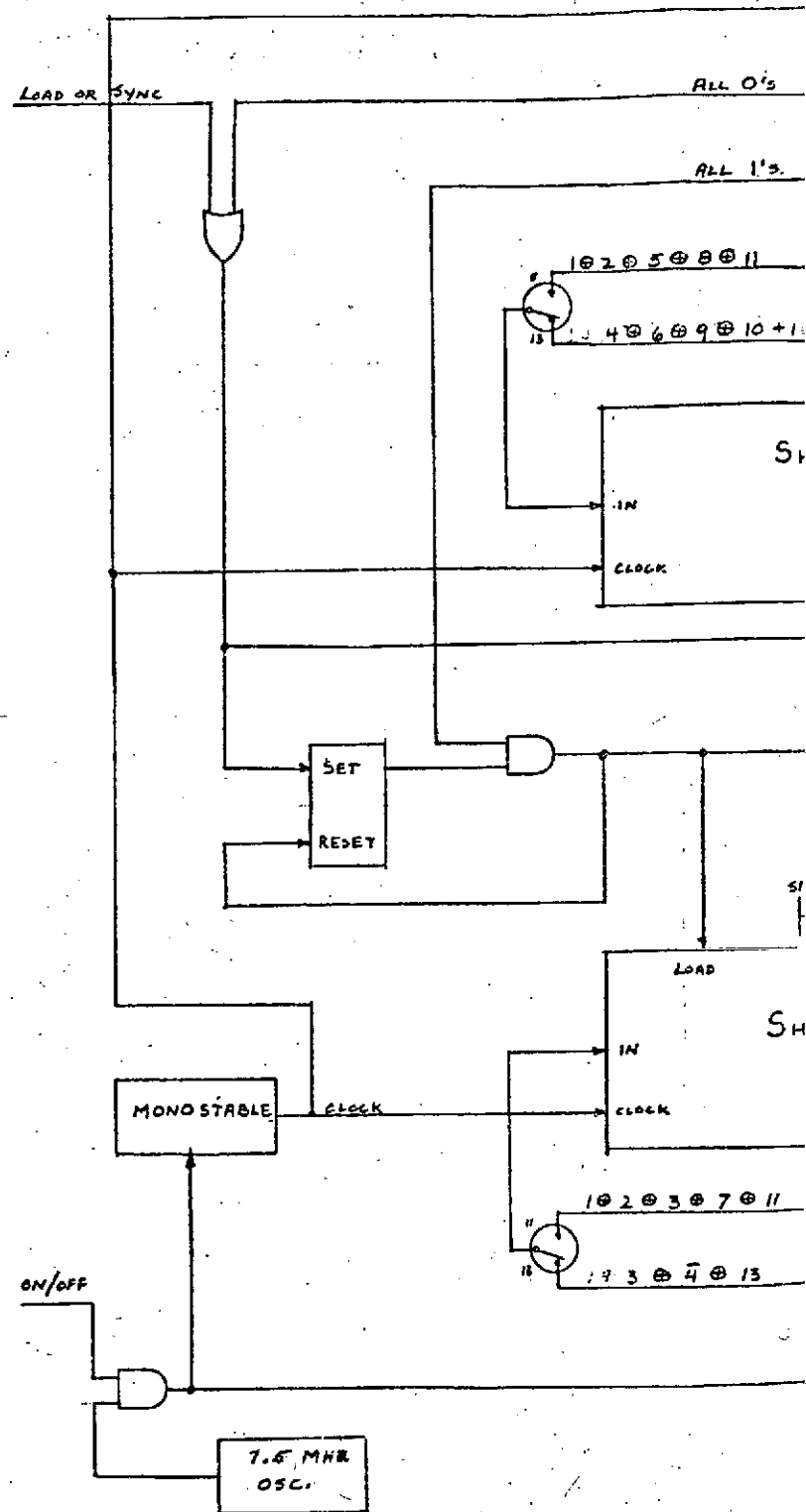


FIGURE 3-3
CODE GENERATOR LOGIC



3-7a

Each register produces a maximal length linear sequence with eleven stages for a 2,047 bit code or thirteen stages for a 8,191 bit code. The number of stages used is selected by the circled switches and implemented by a plug-in connector board with jumpers between the appropriate connector pins. In the 8,191 mode, the A and B register feedback connections to the first stage input are $4 \oplus 6 \oplus 9 \oplus 10 \oplus 13$ and $3 \oplus 4 \oplus 13$, respectively. In the 2,047 mode the A and B register feedback connections to the first stage input are $2 \oplus 5 \oplus 8 \oplus 11$ and $2 \oplus 3 \oplus 7 \oplus 11$, respectively. The module 2 sum of the code sequences from the A and B registers then produce a pseudonoise code which is a member of a Gold code family. If the two codes are shifted in phase with respect to each other a different code results which still belongs to the same Gold code family. For code length of 8,191 bits all the possible combinations result in 8,192 different codes.

The AND gates above register A detect the point in the code when all thirteen (or eleven) bits are one or zero. The all zero state is not a valid state and the detector for all zero state presets the A register to the all one state. The all one state detector is activated once during every 8,191 (or 2,047) bit sequence. This output causes the B register to be preset with an external number which is one of the thirteen bit states in the B register code. When the external number is changed the B code is effectively shifted in phase with respect to the all one state in the A register and a different Gold code results. An external sync pulse may be applied to the code generator. This causes the A register to be immediately preset to the all one state and thereby synchronizes the code generator to an external system.

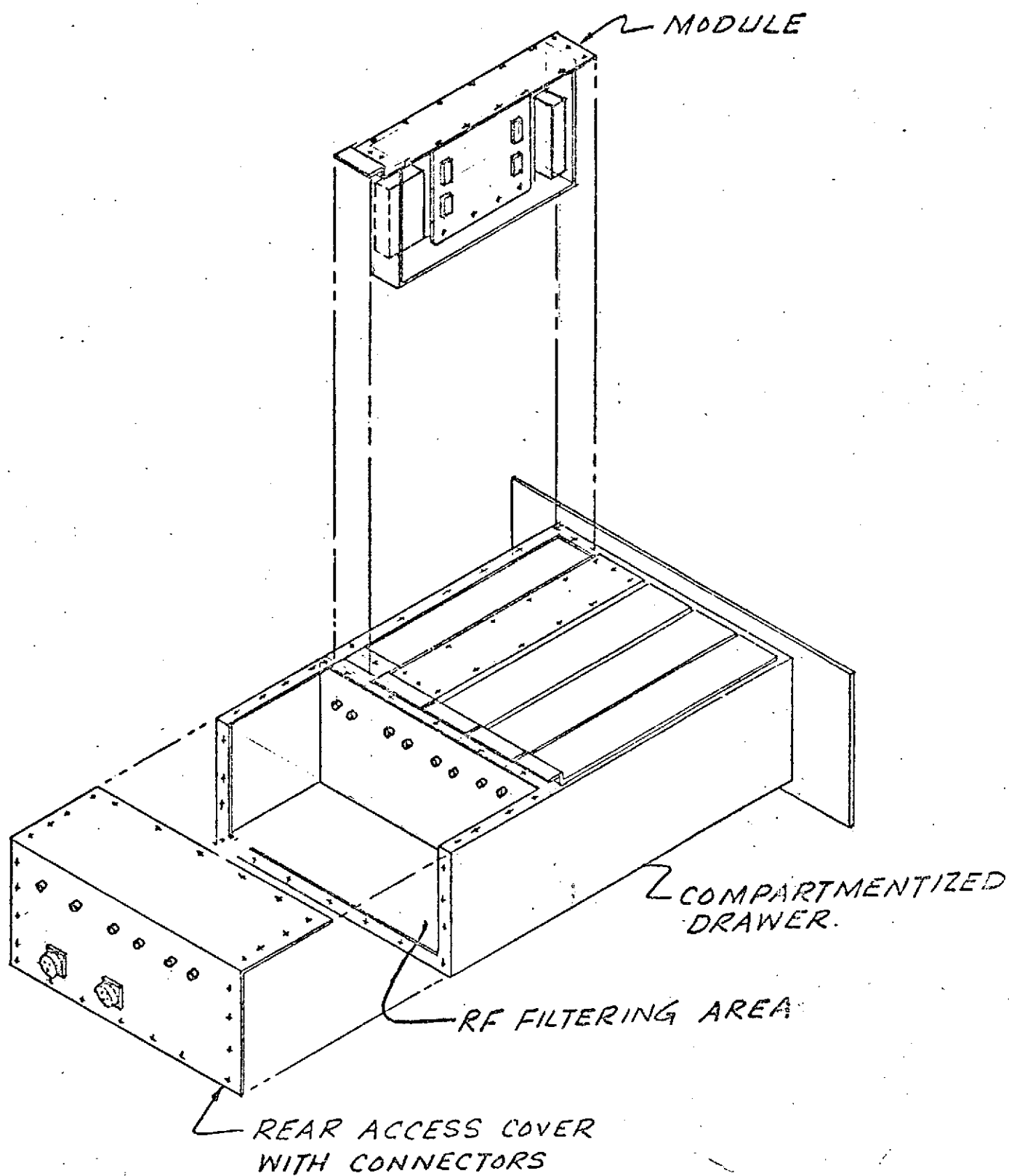
The Gold code is sent to two circuits which control the final outputs. The lower circuit consists of a variable monostable, a delay register and a selector. The monostable delays the clock input by up to one clock period. The delayed clock then gates the code through a two-stage register which has four outputs representing code delays from zero to two bits in one half bit steps. The selector determines which half bit time slot of delay is sent to the output. The second circuit to which the Gold code is sent is the modulation selector. Here the code is mixed with a simulated data input or a square wave at one sixteenth the clock frequency. The code, data, or square wave may be elected as the output without mixing.

The RF level controls for each S-band oscillator source are mounted on the control panel. The maximum power out of each module is -25 dBm, which may be continuously reduced by as much as 50 dB or shut off entirely. The logic mode controls will be mounted on the front of each RFI drawer. A mode select switch allows for manual selection among the following modulation modes: no modulation (i.e., CW), square waves at one sixteenth the system clock rate, data only, PN code only, PN and data, and PN and square waves. The load or "Prep" button cause the PN code to restart when the button is released.

The PSK modulators are microwave integrated circuits mounted on an alumina substrate. Phase shifting is accomplished by employing PIN diode switches to vary the signal line length and thus accomplish quantum time delays equivalent to a $\pm 90^\circ$ in phase shift of the signal. The switches are driven by an interface driver-amplifier which accepts a TTL logic signal as its input.

This modulator design has been selected because standard S-band mixers do not have sufficient isolation to maintain a high value of carrier suppression.

Figure 3-4 typifies the construction of all the assembly drawers to be fabricated in the TDRS Simulation System.



V73-2647

FIGURE 3-4
TYPICAL INTERFERENCE SOURCE ASSEMBLY

3.2 SATELLITE EQUIPMENT

TDRS SATELLITE EQUIPMENT LINKS THE MULTIPLE ACCESS USER TO GROUND STATION. SIMULATED SATELLITE EQUIPMENT DESIGN REFLECTS FLEXIBILITY, ECONOMY AND CLOSE ELECTRICAL CORRESPONDENCE WITH EXPECTED TDRS OPERATION.

As may be seen in Figure 3-5, the simulated TDRS equipment is composed of four major assemblies - they are: the S-band receiver, the multiplexer, the forward link and the satellite frequency sources. The function of the simulated satellite equipment is to accept the outputs of the thirty element S-band helix array and FDM such that they can be relayed via the K_u -band link to the ground. A secondary function of the satellite equipment is to receive a second K_u -band signal from the ground for transmission to the S-band multiple access user. It is in this manner that two-way communication between the multiple access users and the ground station terminal are maintained. In support of these activities the simulated TDRS has been equipped with both a multiplexer frequency assembly and a primary phased locked frequency source. The multiplexer frequency assembly is coherent with a reference from the primary frequency source which in turn is phase locked to a ground station generated pilot.

Each function, assembly and subassembly of the simulated satellite will be detailed in the subsequent subsections. Where the unit or major component is one which is used repeatedly throughout the system, the specifications will be found detailed in Appendix I.

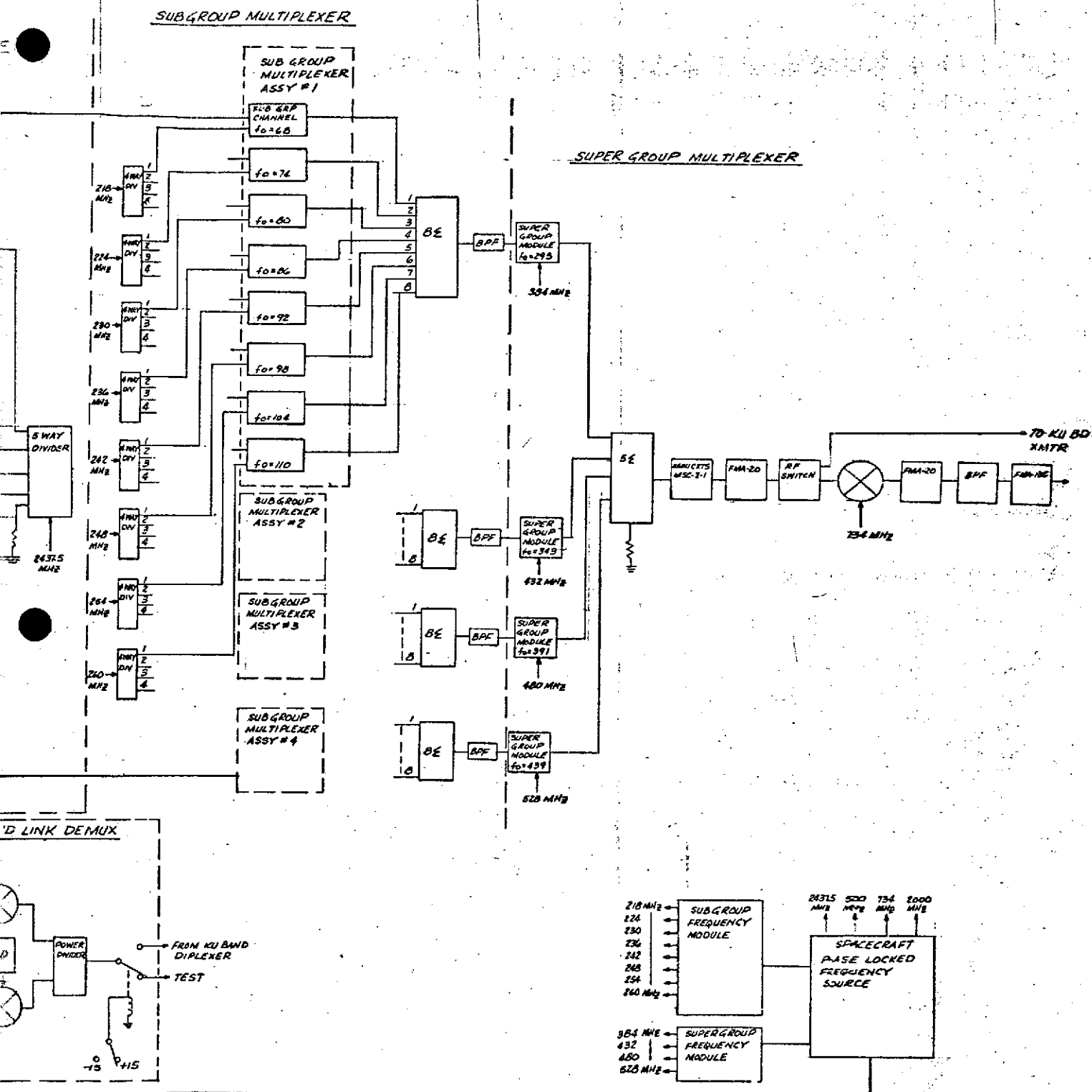


FIGURE 3-5
SATELLITE EQUIPMENT

3.2.1 S-BAND RECEIVER

RECEIVER ASSEMBLY ESTABLISHES SYSTEM SENSITIVITY AND PROVIDES TRANSLATION TO FIRST IF. THE S-BAND SATELLITE RECEIVER ACCEPTS INFORMATION FROM EACH ELEMENT OF THE THIRTY ELEMENT ARRAY AND THROUGH TRANSLATION, FILTERING AND AMPLIFICATION, ESTABLISHES A COMMON 150 MHz IF WITH THE PROPER CHANNEL BANDWIDTH AND LEVEL TO INTERFACE WITH THE MULTIPLEXER UNIT.

The S-band receiver assembly accepts the 30 independent outputs of the multiple access helix array and processes each one independently. This independence in channel processing is maintained throughout the satellite and final combination occurs only after these signals have been retransmitted to the ground station and the adaptive processing has been completed.

The S-band downconverter unit described in Appendix I, accepts the output from each element of the array and translates the S-band spectrum centered at 2287.5 to 150 MHz. A low noise, custom hybrid amplifier (FMA-5022) supplies approximately 40 dB of gain to both raise the level of the signal and establish the system noise figure. The number found within the triangular shaped symbol in Figure 3-6 denotes the accumulated gain over loss ratio up to that point in the system, and is thus employed to insure that the S-band downconverter noise figure is not degraded by subsequent assemblies. The number found within the circle denotes the peak power of the received spectrum at that point in the system. This value is employed by the system designer to insure that intermodulation levels due to component nonlinearities are maintained at least 60 dB below the signal level.

The 150 MHz filter whose detailed specifications were discussed in Section 2.4 and listed in Appendix I follows the S-band downconverter and establishes the channel bandwidth for the S-band receiver. The 150 MHz IF amplifier is a basic 40 dB gain module with the capability of ± 10 dB of adjustable range. This unit is composed of components that reflect the system philosophy of commonality.

The FMA-131 and -135 thin film hybrid amplifiers, the FMA-20 thin film hybrid variable attenuators and the PSC2-1 two-way hybrid power divider are all units employed extensively throughout the system (see Appendix I).

To insure proper operation of each S-band receiver, an RF test point allowing a monitoring access at the receiver-multiplexer interface has been made available. This test point allows for proper setting of the variable gain IF module and quick determination of malfunction.

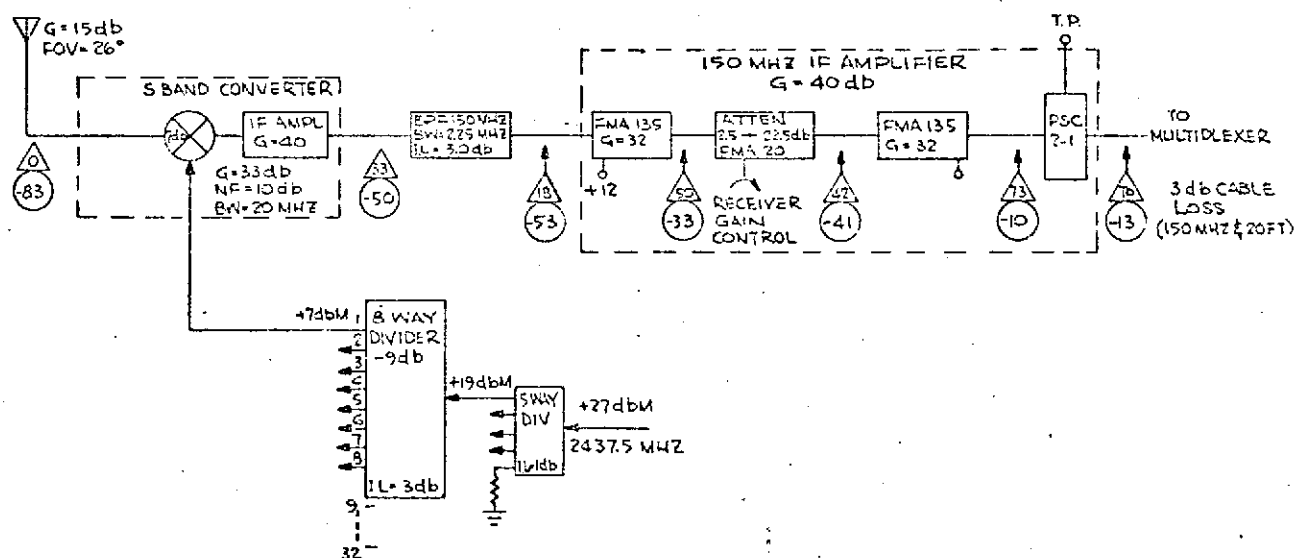


FIGURE 3-6
S-BAND RECEIVER ASSEMBLY

3.2.2 FORWARD LINK

EMPLOYING DATA RECEIVED VIA THE K_u -BAND LINK AND A FREQUENCY SOURCE PHASE LOCKED TO THE GROUND STATION, FORWARD LINK INFORMATION IS RETRANSMITTED COHERENTLY TO THE MULTIPLE ACCESS USER.

Data from the ground station to the multiple access user is retransmitted via the forward link in the satellite. This forward link data in the simulation equipment can originate either as a test signal from the ground station or data from the external K_u -band diplexer. Both of these signals are available by means of an RF switch to the satellite forward link demultiplexer where the data is translated in frequency from 606.40625 MHz to 106.40625 MHz. As shown in Figure 3-7, the multiplexer output is fed to the forward link transmitter. The power level is set by a 1 dB step attenuator, amplified and translated to the output frequency of 2106.40625 MHz. A bandpass filter after the mixer eliminates the undesired mixer cross products. The transmitter output signal is then fed to the single element transmitter antenna.

The input power level to the forward link transmitter at the demultiplexer interface is approximately -44 dBm. A step attenuator is provided to allow a calibrated adjustment of the transmitter output power in one dB steps. The range of this step attenuator will be at least 20 dB and will be manually set.

The amplifier after the attenuator will have a fixed gain of approximately 33 dB. The maximum amplifier output power of approximately -12 dBm will ensure that the amplifier will not be operated near saturation. The amplifier has a one dB compression point of +9 dBm and a third order intercept point of +22 dBm.

The double balanced mixer will generate the desired transmitter frequency of 2106.40625 MHz. Other products will be removed by the output bandpass filter. The shape factor of the filter is determined primarily by the 60 dB of isolation required at the image frequency of 1893.59375 MHz and at the L.O. frequency of 2000 MHz. This requires a filter with a 3 dB bandwidth of 20 MHz or greater with at least four sections and approximately a 1% bandwidth. Tubular filters at this

frequency and bandwidth would have intolerable insertion losses. An interdigital filter will therefore be used for this application.

The amplifier employed in this circuit possesses a third order intercept point of ± 22 dBm. The intermodulation products in this amplifier must be kept at least 60 dB below the desired transmitter signal. Since the maximum desired signal is approximately -12 dBm an additional equal amplitude interference signal would generate intermods that would be at least 66 dB below the desired transmitter signal. The multiplexer output will therefore not contain any spurious or interference signals that are within 60 dB of the desired signal.

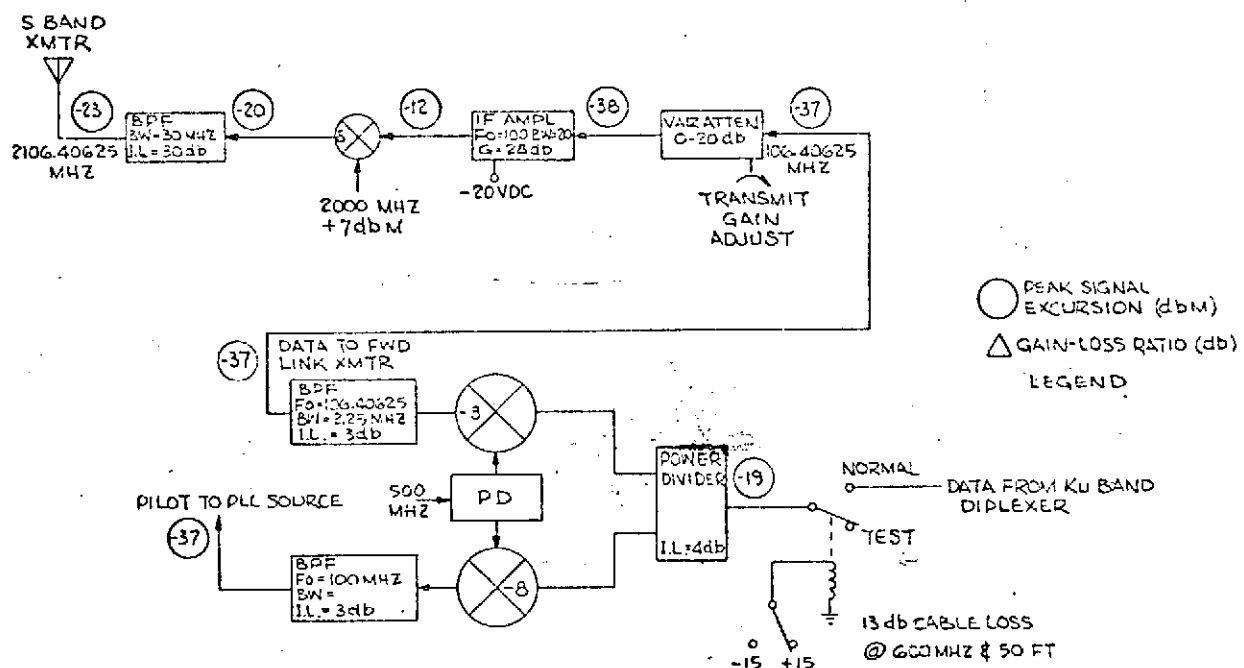


FIGURE 3-7
SATELLITE FORWARD LINK

3.2.3 SPACECRAFT MULTIPLEXER

THE TDRS MUST TRANSMIT TO THE ADAPTIVE PROCESSING GROUND STATION THE THIRTY INDEPENDENT OUTPUTS OF THE S-BAND MULTIPLE ACCESS ARRAY. A DESIGN HAS BEEN IMPLEMENTED THAT PRESERVES ELEMENT INTEGRITY AND MINIMIZES SIGNAL DEGRADATION DUE TO CROSS TALK AND PHASE NONLINEARITIES.

The function of the spacecraft multiplexer is that of accepting the thirty individual outputs from the S-band multiple access array and generating an FDM spectrum for retransmission via the K_u -band link to the ground station. In order to accomplish this and yet maintain the integrity of each of the thirty channels, it is necessary to implement a two-step FDM process. Because there are thirty channels, each of which must maintain its electrical relationship with the others, it is not possible to both upconvert and filter in an equal manner in a single step. That is, a filter designed for the proper bandwidth/phase slope relationship for the lowest center frequency channel would when translated to the highest center frequency channel be generally unacceptable due to the inherent shrinkage of the filters linear phase bandwidth. The two-step multiplexing scheme is accomplished in the subgroup and supergroup multiplexer assemblies respectively.

The Subgroup Multiplexer assembly, shown in Figure 3-8, accepts the thirty down converted 150 MHz IF signals from the S-band receiver assembly and immediately translates each signal to one of eight subgroup channel frequencies. Each subgroup consists of eight channels whose center frequency ranges from 68 to 110 MHz in 6 MHz ascending steps. Thus, four subgroups are required to properly process thirty channels. Each channel is independently down converted by means of a standard double balanced mixer to its proper channel frequency. Each channel in turn possesses independent gain (FMA-135), gain control (FMA-20), band pass filtering and a channel monitoring point. The hybrid amplifier and gain control device, the FMA-135 and FMA-20 respectively, are the Fairchild units described in Appendix I. Once again both units are being utilized well below their maximum linear operating points to insure low intermodulation products. The individual channel monitoring point allows for both independent channel observation and the opportunity to operate multiplex and demultiplex subassemblies in a back-to-back fashion.

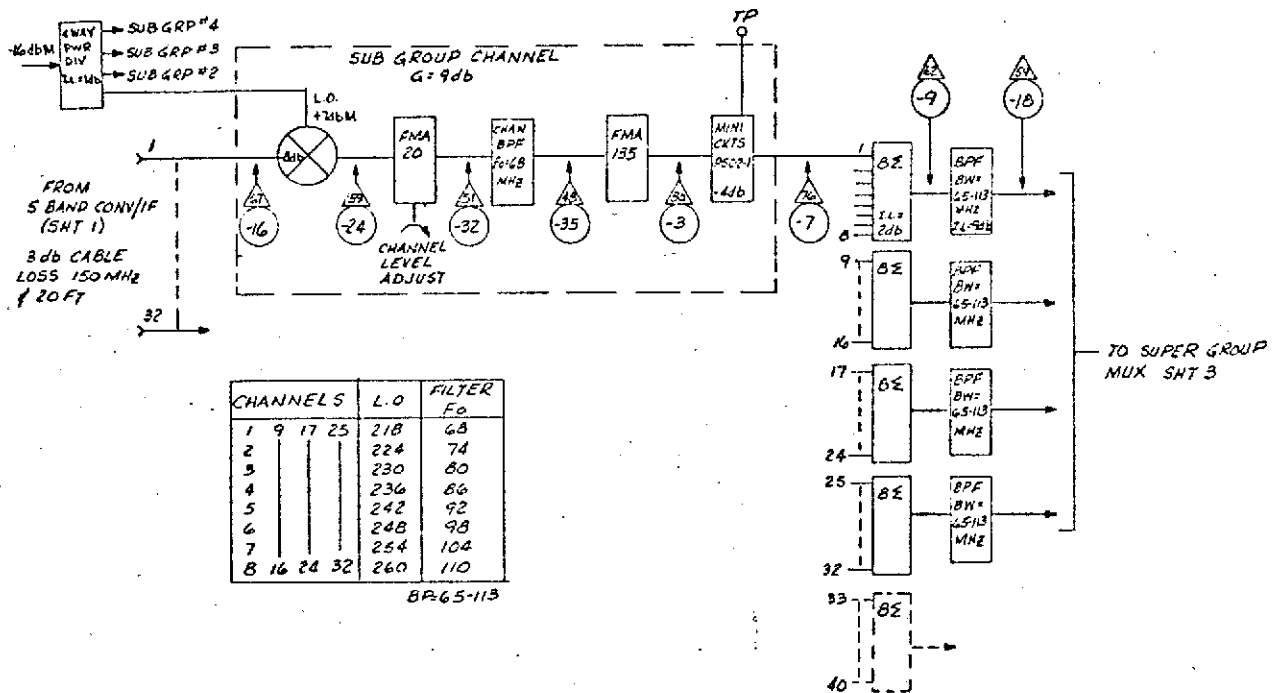


FIGURE 3-8
SUBGROUP MULTIPLEXER ASSEMBLY

The subgroup channel filters have been selected to both satisfy the rejection requirements for the channel L.O.'s 218 through 260 MHz and at the same time not alter the phase tracking specifications set down by the S-band receivers narrow band IF filter (see Appendix I, System Filter Specifications, spec # 1002).

Each of the eight frequency offset channels are combined in an 8-way summer, thus forming a single 48 MHz wide subgroup spectrum. This signal is filtered to further reduce spurious signals outside the subgroup spectrum and passed to the Supergroup Multiplexer assembly.

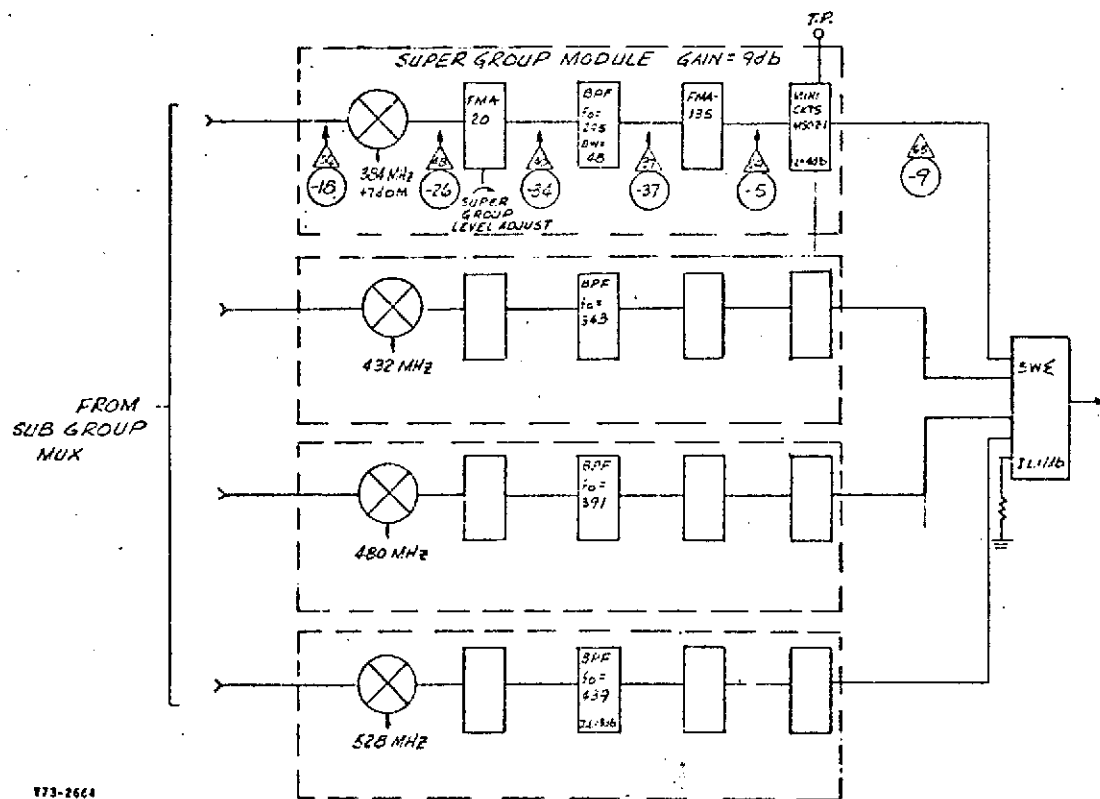
The Supergroup Multiplexer assembly, shown in Figure 3-9, accepts the four 8 channel 48 MHz wide subgroup signals and forms a single 192 MHz FDM aggregate signal at the proper level to interface with the K_u -band transmitters. In addition, this assembly also makes available for system testing an inverted multiplexer spectrum for direct interface with the ground station demultiplexer. Selection of "normal" or "test" mode shall be made by access to the rear panel and implemented by means of an RF switch.

The selection of the supergroup frequency bands was chosen so as to both be high enough in frequency to make for easy translation to K_u -band and yet be strategically located so as to not be overlapped by any frequencies employed by the preceding subgroup assembly.

One possibly interfering signal occurring in the supergroup assembly is that of the adjacent L.O. signal leakage (see Appendix III). Because adjacent supergroup L.O.'s fall within the passband of the upper supergroup spectrums, additional L.O. isolation in the form of additional filtering on each L.O. line is required. Additional isolation (i.e., above the 60 dB isolation specified for the supergroup frequency module) is supplied by adjacent L.O. rejection of 60 dB by the individual L.O. filters.

The supergroup filters, like those described for the subgroup, are designed to provide the rejection of known interfering signals (i.e., L.O.'s, images, etc.) and yet not impair the phase tracking specifications established at the S-band receiver. The remainder of the components are standard system components whose electrical specifications have been discussed.

By the proper distribution of low noise hybrid amplifiers in both the sub and supergroup assemblies, the minimum gain/loss ratio for the TDRS is maintained above a level of 5,000 (37 dB) which preserves the S-band receiver front end noise figure.



173-2664

FIGURE 3-9A
SUPERGROUP MULTIPLEXER ASSEMBLY

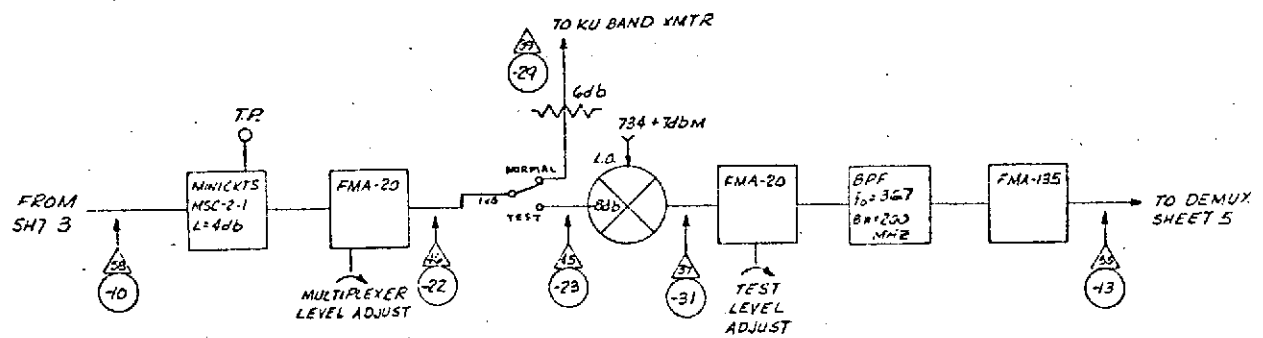


FIGURE 3-9B
SUPERGROUP MULTIPLEXER ASSEMBLY

3.2.4 SATELLITE FREQUENCY SOURCE

ASSEMBLY ACQUIRES GROUND GENERATED PILOT AND COHERENTLY SUPPLIES ALL REQUIRED SATELLITE FREQUENCIES.

The function of the satellite frequency source is to supply all of the frequencies required by the TDRS for signal processing. To accomplish this the frequency source supply function is split amongst three frequency generating subassemblies. There is a first, the phase locked frequency source which makes the required acquisition of the forward link pilot and generates the required S-Band Receiver L.O.'s. In addition, there are the two assemblies needed to supply the multiplexer assembly, with its required multiple L.O. frequencies. These two assemblies are the super and subgroup frequency modules, respectively.

The phase locked frequency source's narrow band phase locked loop supplies coherency with the ground by making acquisition with a 600 MHz ground station generated pilot. It is on the basis of the acquisition of this pilot that the phase locked frequency source supplies in a coherent fashion the required S-band L.O.'s and the needed super and subgroup reference frequencies. The super and subgroup frequency modules accept their reference frequencies from the phase locked frequency source and in a coherent fashion supply the required multiplexer L.O. frequencies.

The following sub sections shall give a detailed explanation of the three assemblies mentioned above that make up the satellite frequency source.

3.2.4.1 PHASE LOCKED FREQUENCY SOURCE

UNIT ACQUIRES 600 MHz PILOT SIGNAL AND COHERENTLY PRODUCES REQUIRED TDRS FREQUENCIES.

The phase locked frequency source seen in Figure 3-10 is composed in the main of modified sections from the AGIPA feasibility program. The heart of the present phase locked source is a very low gain voltage controlled crystal oscillator. In order for this unit to provide its required frequencies such that they are coherent with the ground station the 5 MHz VCXO must make acquisition with, and hold lock onto, a pilot

received from the ground. It is assumed that this pilot arrives at the TDRS with a very high carrier to noise ratio (CNR).

Since the VCXO presently in the phase locked source is available for use and no particular specifications other than not adding to the phase noise already present on the received pilot exist, there appears no reason not to employ this device.

Employing this 5 MHz VCXO unit does, because of its low gain, incur some limitation on the loop which must be determined first. The measured gain of the VCXO is one part per million per volt. In effect then, K_o , the VCXO gain, for the 5 MHz VCXO is equal to 10^{-6} radians/volt. The maximum control voltage range of this unit is plus or minus five volts. It is assumed that K_d , the phase detector gain, would be approximately 50 millivolt/radian, a reasonable value for a standard double balanced mixer employed as a phase detector, then the maximum non-saturating DC gain in the loop is equal to 100. To determine then, K_v , the maximum open loop gain, the following is computed:

$$K_v = \alpha K_d K_o N A$$

where,

α = limiter losses

and N = multiplying factor applied to VCXO

Since the signal to noise ratio of the pilot will be high α , the limiter loss, may be assumed equal to one. The multiplying factor for the loop shown in the Figure is computed as follows:

$$N = N_1 + N_2 + N_3 - N_4 - N_5$$

where N_1 = multiplication to 14.0 GHz

N_2 = multiplication to 500. MHz

N_3 = multiplication to 100. MHz

N_4 and N_5 = multiplication to 2.5 MHz

therefore,

$$N = 2919$$

Using this value for N and the maximum unsaturated DC gain permissible Kv is determined:

$$K_v = (1.0) \left[50 \text{ mv/rad} \right] \times \left[2\pi \times 5.0 \text{ rad/volt} \right] \times 2919 \times (100)$$

which equals

$$k_v = 4.59 \times 10^6$$

If it is assumed that over the tracking range considered acceptable the phase error should be limited to 0.1 radian then the maximum tracking range may be determined as follows:

$$= \frac{W}{K_v} \quad \phi_e = \frac{\Delta \omega}{K_v}$$

and thus

$$= 0.1 K_v \quad \Delta \omega = 0.1 K_v$$

or

$$= 4.59 \times 10^5 \quad \Delta \omega =$$

which is equal to 73.0 KHz at Ku-band.

With the tracking range established for the given VCXO specifications the next loop parameters to be determined are the loop natural frequency and damping factor. Since the received pilot is to be found well above the noise level for bandwidths on the order to two megahertz there is ample signal available for large loop bandwidths. The limitation on loop bandwidth rather than signal to noise ratio will depend more upon the required rejection of the 2.5 MHz reference by the loop filter. Assuming 60 dB of rejection, plus a 6 dB margin, to be sufficient, 2.5 MHz attenuation limits the natural loop bandwidth to approximately 4000 radians. The loop noise bandwidth then for a damping factor of 0.5 equals 2000 Hz. The damping has been chosen equal to 0.5 to achieve the optimum Doppler tracking in the loop.*

* Gardner, F. M. "Phase lock Techniques."

The approximate lock range of the loop with the loop natural frequency stated above is 640 Hz. The pull in range and time will be on the order of 40 KHz and 0.25 second, respectively. No acquisition scheme is envisioned for this unit as it has been assumed that the received signal will be positioned to appear within the acquisition range of the loop.

Once loop acquisition has occurred, the generation of the units' required frequencies is quite straightforward. The output of the basic 5 MHz VCXO, now phase locked to the incoming pilot, is used through a series of multipliers to generate 100 MHz. This 100 MHz signal in turn drives a step recovery diode (SRD) spectrum generator which in a comb-like fashion produces signals at 100 MHz intervals up through one GHz. A pair of x 5 multipliers in conjunction with products of the basic 5 MHz source produce the required S-band frequencies.

3.2.4.2 MULTIPLEXER FREQUENCY SOURCE

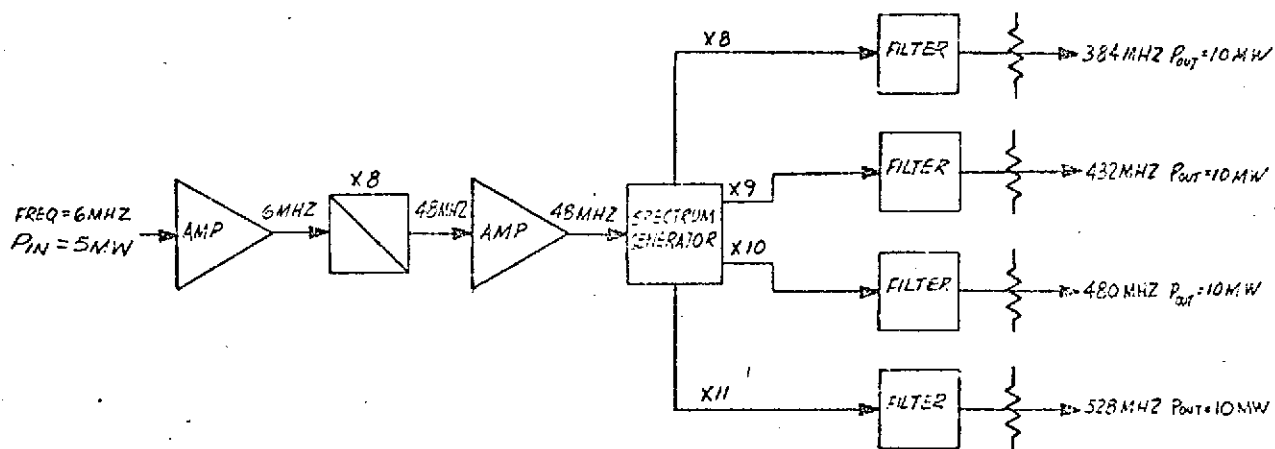
THE SUPER AND SUBGROUP FREQUENCY SOURCES EMPLOY TWO REFERENCE FREQUENCIES FROM THE PLL FREQUENCY SOURCE TO GENERATE THE FOUR SUPER GROUP AND EIGHT SUBGROUP FREQUENCIES REQUIRED BY THE MULTIPLEXER.

The supergroup frequency module displayed in Figure 3-11 accepts a 6.0 MHz reference frequency from the phase locked frequency source and in a straight x 8 multiplication produces 48 MHz. This signal is subsequently fed to a SRD spectrum generator and the appropriate signal is selected by band pass filtering.

The subgroup frequency module shown in Figure 3-12 accepts a 6.0 MHz and a 200 MHz reference signal from the phase locked frequency source. These two reference signals are employed to lock up eight similar but offset phase locked loops. Each loop is offset 6 MHz. Each loop employs MECL 10,000 series logic to prescale the difference frequencies in each loop so that the same 6 MHz may be employed as a reference.

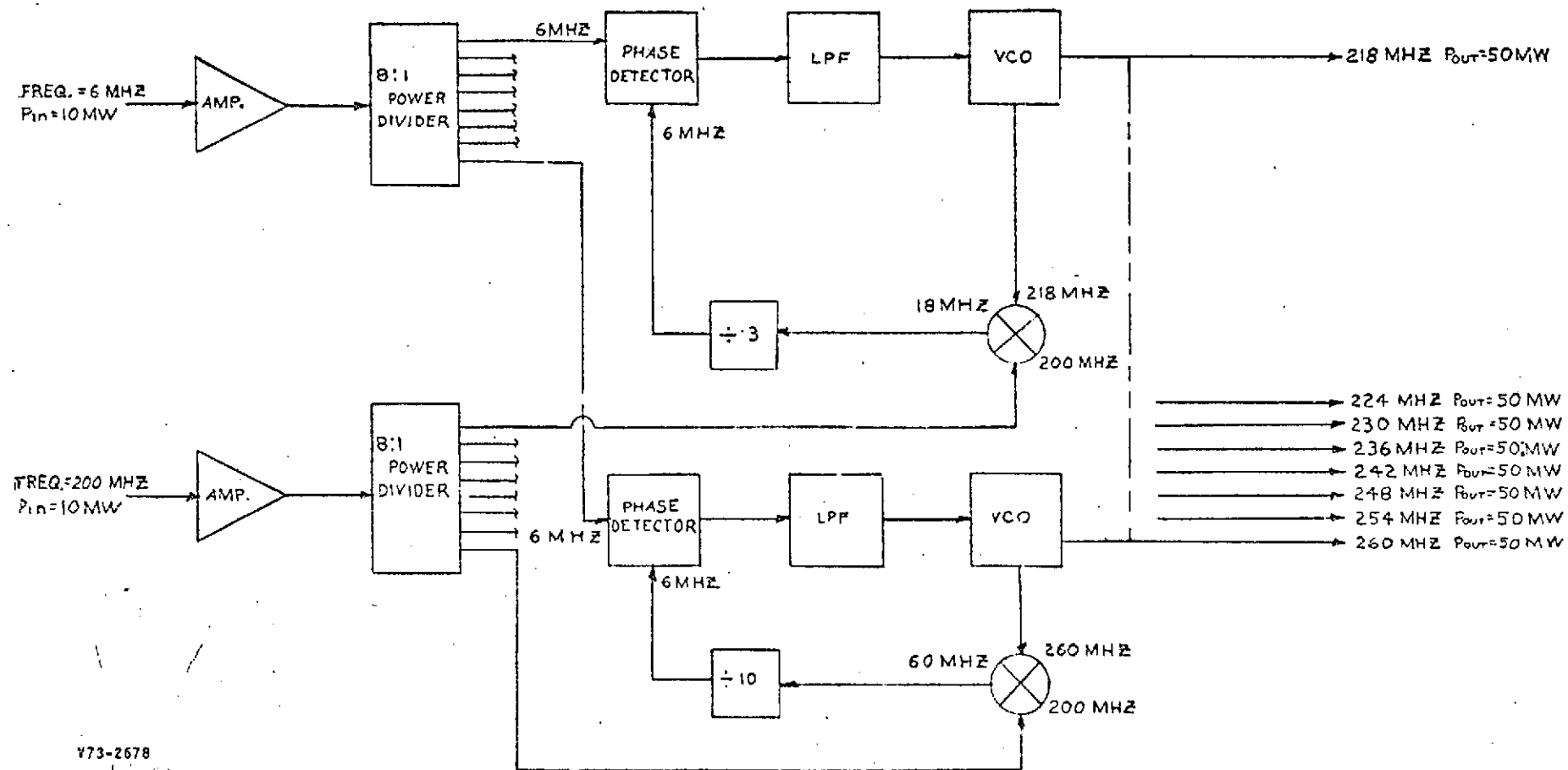


3-29



173-2679

FIGURE 3-11
SUPERGROUP FREQUENCY MODULE



Y73-2678

FIGURE 3-12
SUBGROUP FREQUENCY MODULE

3.3 GROUND EQUIPMENT

GROUND STATION EQUIPMENT ACCEPTS THE FDM SIGNAL FROM SATELLITE AND FORMS ADAPTIVE BEAM. ACCEPTING THE WIDE-BAND FDM SIGNAL FROM THE K_u -BAND RECEIVER THE GROUND STATION DEMULTIPLEXES THE THIRTY INDIVIDUAL CHANNELS AND THEN, THROUGH THE SYSTEM COMPUTER, WEIGHTS THEM IN AN OPTIMUM SIGNAL TO INTERFERENCE PLUS NOISE SENSE.

The ground station assemblies are shown in Figure 3-13. The first assembly that the signal passes through is the demultiplexer unit which, in a two-step process, converts the 30 individual components. The individual components are then passed on to the RF processing assembly which splits the signal into an unweighted sample and a "weighted" 30 channel sum. The weighting of each channel occurs in the RF processing assembly where each subassembly processes eight channels, "weights" and sums them, and sends them on to the Digital Processor.

The Digital Processor accepts both the sampled and the summed signals and extracts both power level and cross correlation values from the thirty channels. The system computer in turn monitors these values and by employing the system algorithm computes new weights to be applied at the RF processing assembly.

The user transmitter simulates the desired user and contains its own code generator. The control unit supplies data for the desired user transmissions. The control unit also directs the power level of the interference sources found in the scenario assembly. The ground station frequency source supplies all of the frequencies required by the ground station assemblies.

All of these units and functions will be discussed in detail in the following sections.

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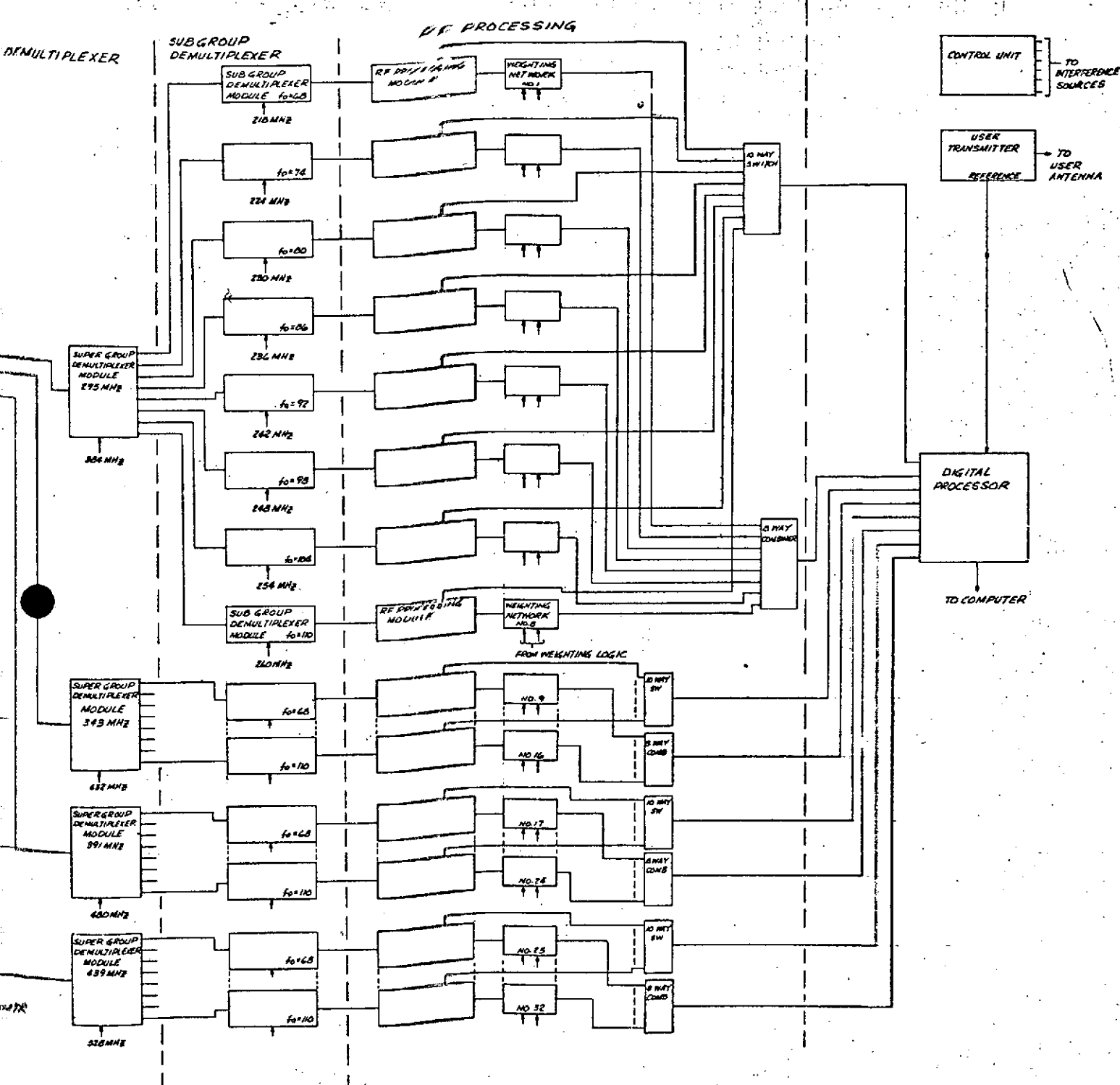
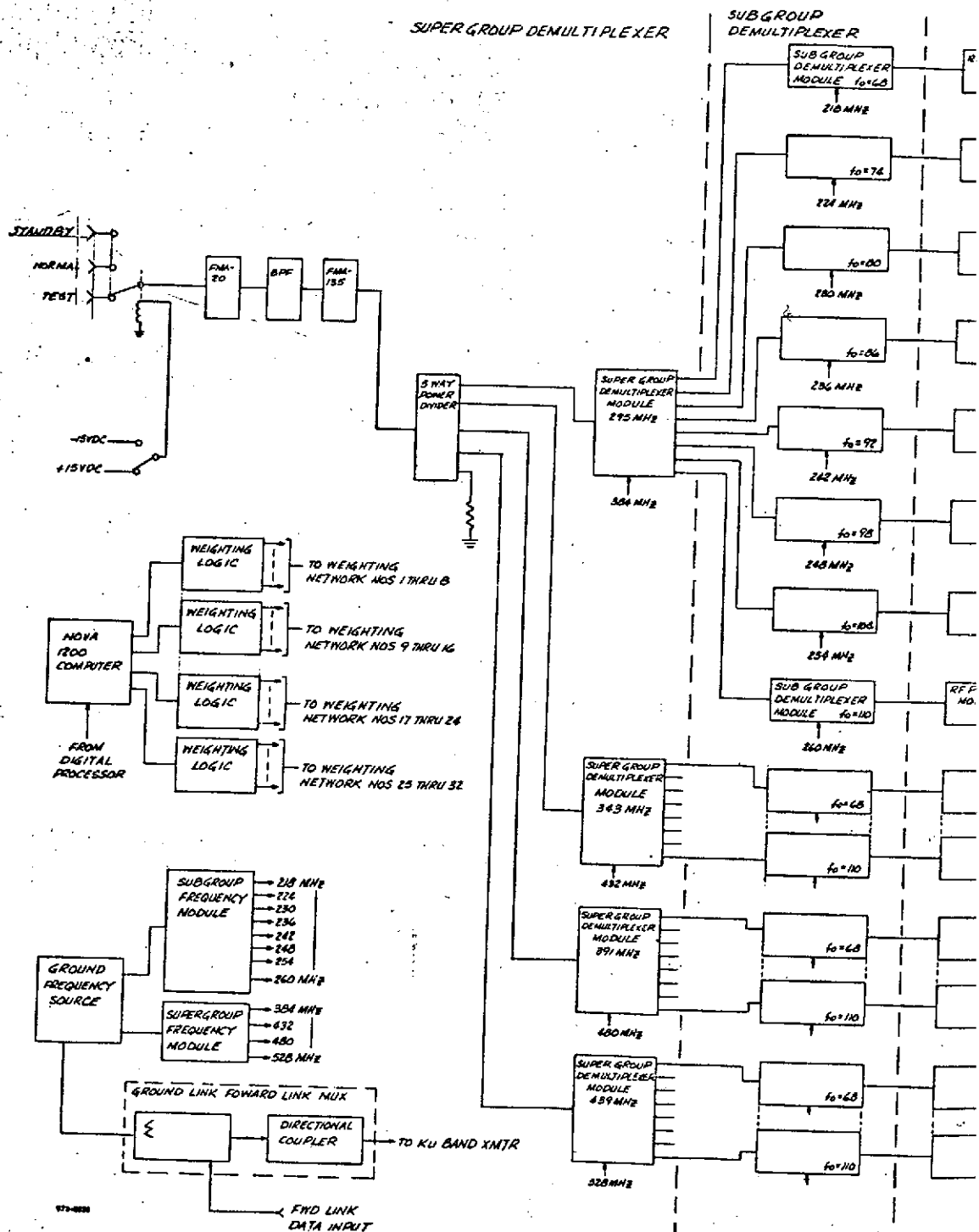


FIGURE 3-13
GROUND STATION EQUIPMENT

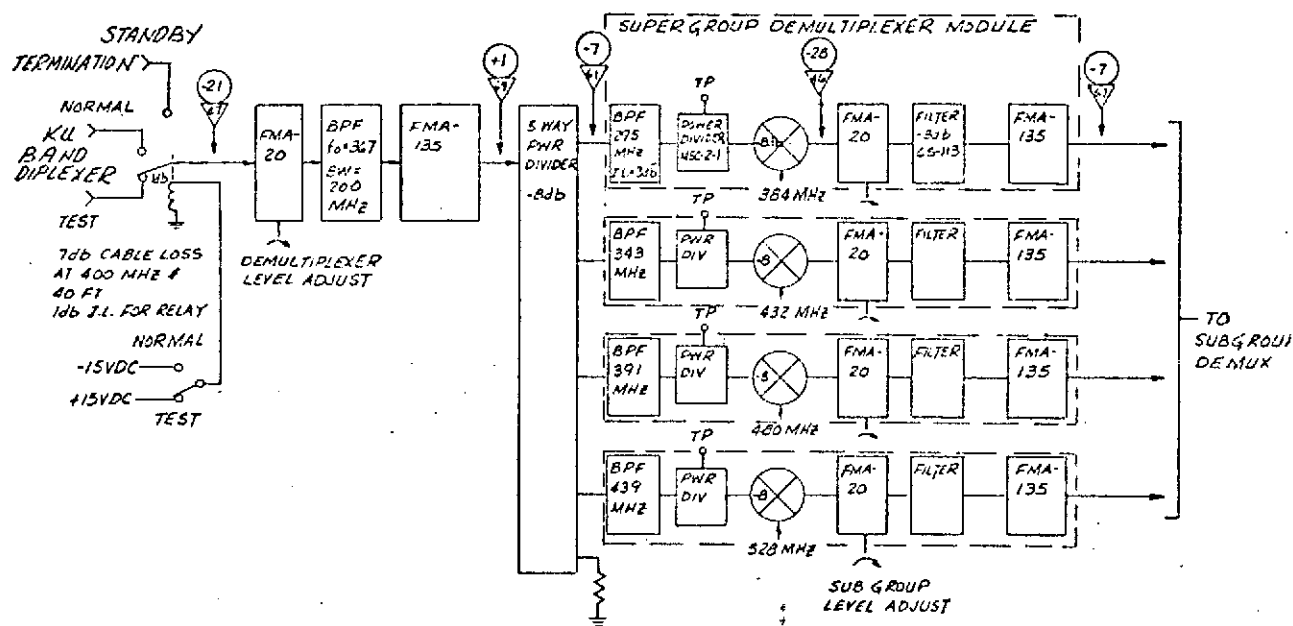


3.3.1 DEMULTIPLEXER ASSEMBLY

THE DEMULTIPLEXER ASSEMBLY MUST RECOVER FROM THE S/C GS K_u -BAND LINK THE 30 SIGNAL OUTPUTS OF THE S-BAND MULTIPLE ACCESS ARRAY. A DESIGN HAS BEEN IMPLEMENTED THAT RECOVERS THE ORIGINAL SIGNALS WHILE STILL PRESERVING THE CHANNEL PHASE AND ISOLATION SPECIFICATIONS ACHIEVED WITHIN THE TDRS.

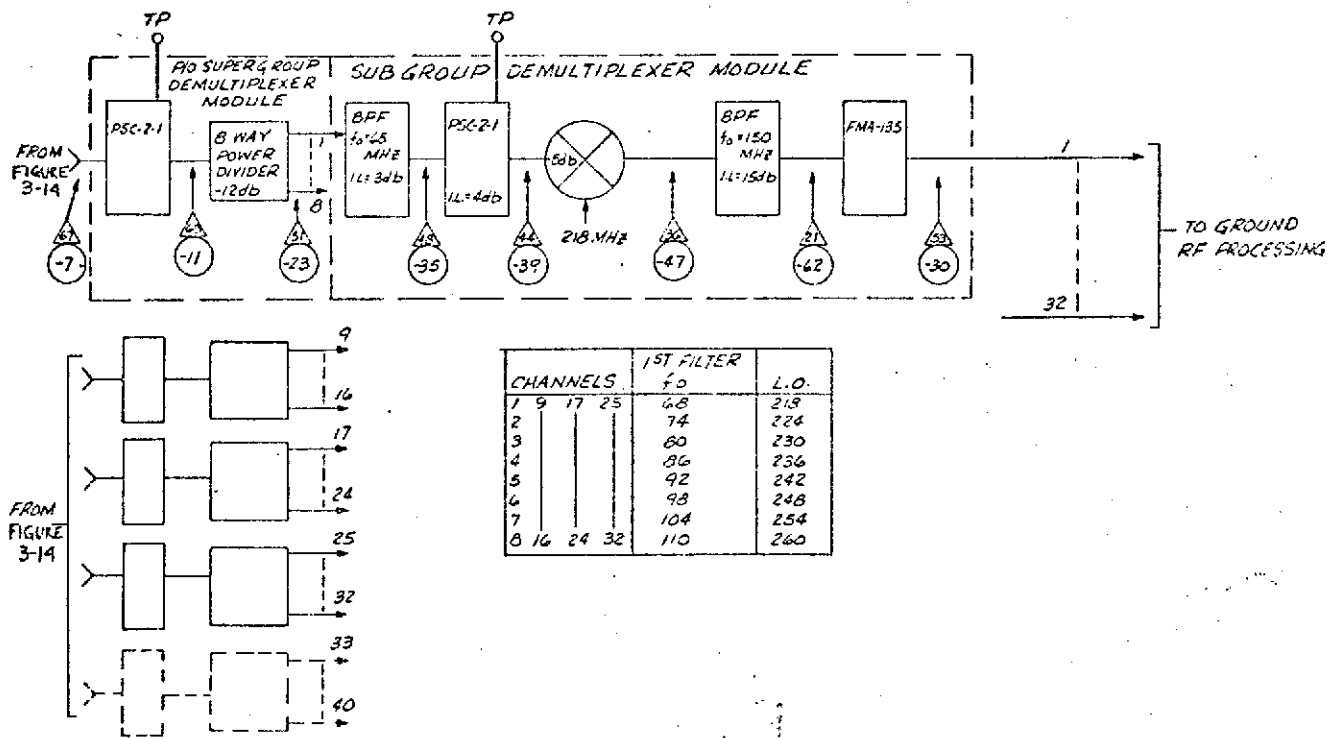
It is the function of the ground station demultiplexer assembly to dismantle the composite signal structure, created by the S/C multiplexer, back into its original components. In much the same fashion, except in reverse order, as described in section 3.2.2.3 for the S/C multiplexer, the demultiplexer assembly accepts the composite 192 MHz 30 channel FDM signal and produces at its output 30, 150 MHz individual signals each related on a one-to-one basis with an element of the S-band array.

The composite 30 channel signal from the K_u -band ground station receiver is first accepted by the supergroup demultiplex assembly. As may be noted in Figure 3-14, the signal is first routed through an RF switch which in the "normal" mode passes the K_u -band receiver output directly to the supergroup and in the "test" mode connects the ground station directly to the output of the S/C multiplexer assembly. This switch allows for back-to-back testing of the multiplexer-demultiplexer assembly and a rapid return to normal operation with the K_u -band link. The input level to the demultiplexer assembly is controlled by means of a variable level adjust and is expected to be -21 dBm peak. The input spectrum from the K_u -band ground station receiver is filtered to remove any undesired spurious signals and subsequently distributed to the four supergroup demultiplexer modules. The proper portion of the wideband spectrum is selected by each supergroup bandpass filter. This signal is then converted by means of the proper supergroup L.O., to the basic subgroup band (i.e., 65-113 MHz). This down converted signal is then filtered (see specification #1003 Appendix I), amplified and power divided to the individual subgroup demultiplexer modules as shown in Figure 3-15.



178-2662

FIGURE 3-14
SUPERGROUP DEMULTIPLEXER ASSEMBLY



V73-2661

FIGURE 3-15
SUBGROUP DEMULTIPLEXER ASSEMBLY

Each subgroup module selects its proper portion of the spectrum by means of the appropriate bandpass filter (see specification #1002 Appendix I), and after allowing for a monitoring point, translates each subgroup channel to a common 150 MHz IF. This signal is further filtered to remove both spurious signals and to once again establish the channel bandwidth.

3.3.2 RF PROCESSING ASSEMBLY

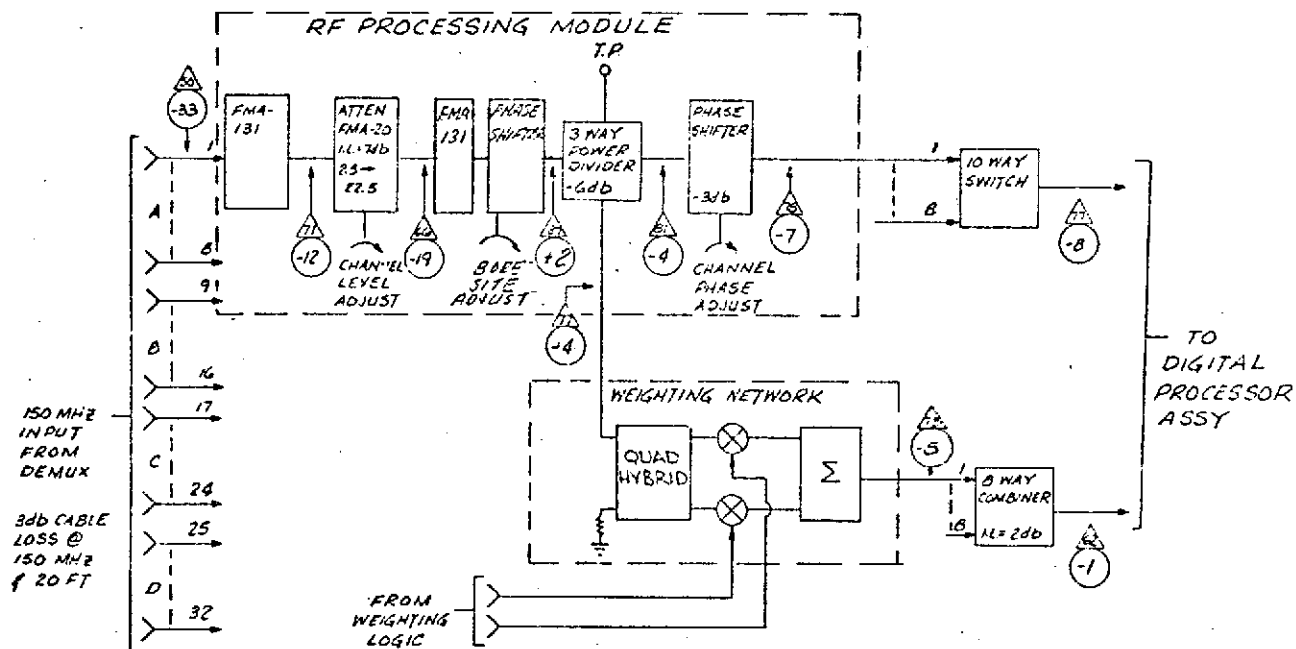
EACH ASSEMBLY SUPPLIES AN EIGHT-CHANNEL WEIGHTED SUM AND AN UNWEIGHTED SAMPLE. UNDER DIRECTION OF THE NOVA 1200 COMPUTER EACH RF PROCESSING ASSEMBLY SUPPLIES AN UNWEIGHTED SAMPLE SIGNAL AND WEIGHTED SUM OF ALL THE CHANNELS IN EACH DRAWER (8).

As may be seen in Figure 3-16, which depicts a single channel of the RF processing assembly, each channel consists of two major subassemblies. That is, the RF processing module and the weighting network module.

The RF processing module consists of a pair of FMA-131 amplifiers, an FMA-20 hybrid attenuator, a three-way power divider and two electronically controlled phase shifters. The two amplifiers and the attenuator are fully described in Appendix I. Their function is to provide a nominal 35 dB of gain with the variable attenuator employed, when necessary, to make up for any level variations. The three-way power divider allows for three equal signal level components. One component of the three-way split is sampled by a computer controlled RF switch and becomes the "sampled" signal. The second component is processed by the weighting network and is eventually summed to yield the "sum" weighted output. The third signal component is brought to an RF test point for system monitoring purposes. The two phase shifters are identical, but employed for different purposes. The phase shifter preceding the three-way hybrid divider is employed to boresight the array and this adjustment should only occur during system set up. The second phase shifter equalizes the phase shift experienced by the "sampled" and "summed" signals encountered enroute to the correlator unit.

Here, as in the remainder of the system, the dynamic range and noise figure of the system, once set, is preserved.

The channel weighting network is unlike that previously employed on the AGIPA system, where a phase shifter and attenuator were employed, in that, instead of a ρ/θ (rho/theta) configuration the generator accepts directly a x/y (real/imaginary) configuration. The incoming signal from the three-way divider is power split in a quadrature hybrid and then each component is processed by an amplitude modulator and then recombined.



973-2656

FIGURE 3-16
RF PROCESSING ASSEMBLY

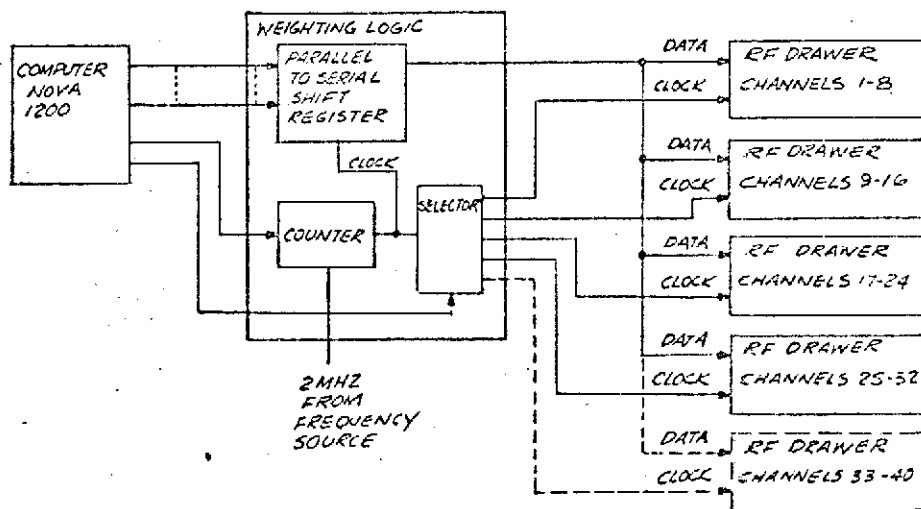
The amplitude modulator is a high level double balanced mixer which because of its nature can not only attenuate the incoming signal but can also change its polarity sign. Thus the recombined output signal can vary the full 360° as well as be attenuated on the order of 30 dB.

Each assembly also contains a weighting logic module, shown in Figure 3-17, to control the eight weighting units within each drawer.

The digital processing assembly sends digital weights to the RF channels through this logic unit. To minimize the number of interrack cables, data is sent in serial format.

When the weights for a single RF channel are calculated, the 16 bits (8 for the real component and 8 for the imaginary component) are loaded from the computer into two parallel-in, serial-out 8-bit shift registers. Sixteen clock pulses are then sent, shifting the data out the serial port in synchronization with the clock. When the proper channel is enabled, it alone receives the clock necessary to shift in the data.

Shift registers in the RF channels receive the new weights, but do not load the channels until a separate computer command is received. Then all channels are loaded with the new weights synchronous with the next data bit. This technique minimizes the transition time for channel weights and minimizes the chance of bit detection errors caused by changing weights.



173-2652

FIGURE 3-17
COMPUTER CONTROLLED WEIGHTIN NETWORK

3.3.3 DIGITAL PROCESSING ASSEMBLY

MULTICHANNEL 150 MHz INPUT PROCESSED UNDER COMPUTER CONTROL. ACCEPTING BOTH "SUMMED" AND "SAMPLED" OUTPUTS FROM THE RF PROCESSING ASSEMBLIES CROSS-CORRELATION AND LEVEL MEASUREMENTS FORM THE BASIS FOR FUTURE COMPUTER ACTION.

As shown in Figures 3-18A and B, the 150 MHz sum outputs of the 8 channel/group RF processing assembly are combined within a five way summer in this assembly. Similarly, any of the 150 MHz sampled outputs of the RF channel groups are selected by an RF switch in this unit. Directional couplers provide test points for these signals. A pair of double balanced mixers with a 160.7 MHz LO converts the sum and sampled signals to 10.7 MHz. Employing bandpass and band reject filtering the "summed" and "sampled" lines are each separated into their signal and interference components. Power detectors measure the signal and interference levels in the summed line. Cross-correlations measurements are made between the "summed" line and each individual "sampled" channel for both the signal and the interference spectrums. These power and cross-correlation measurements result in analog voltages that are the basis for the computer calculations.

The computer reads in the data by means of an analog multiplexer and an 8-bit A/D converter. Computer output to the system is made through logic circuitry. A teletype is also provided for operator instructions and printout of data during testing.

The Nova 1200 computer contains 8K words of core memory. It is equipped with a high-speed floating point processor. This processor provides a great increase in speed for the execution of arithmetic calculations.

A front panel control will be provided for the selection of any RF channel. Implementation of this front panel control overrides the normal computer control of the channel sampling selection, and allows for the monitoring of the cross-correlation values of the selected channel against the weighted "sum."

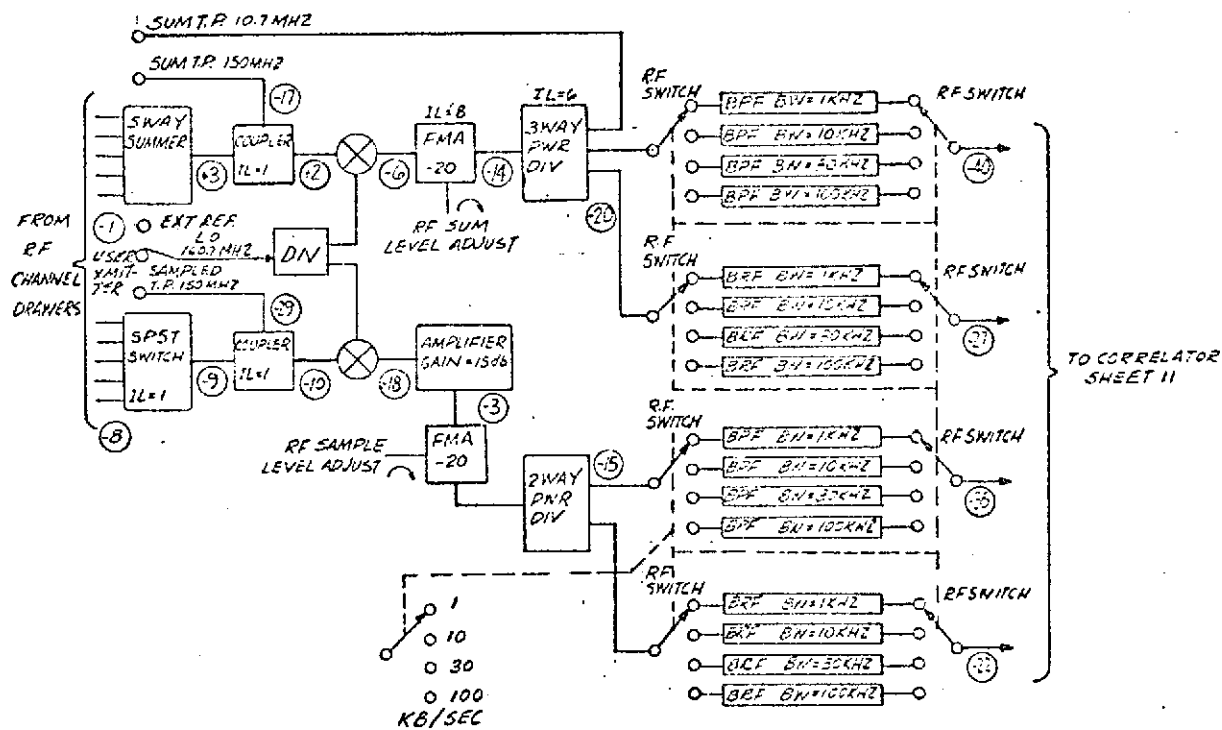


FIGURE 3-18A
DIGITAL PROCESSING ASSEMBLY

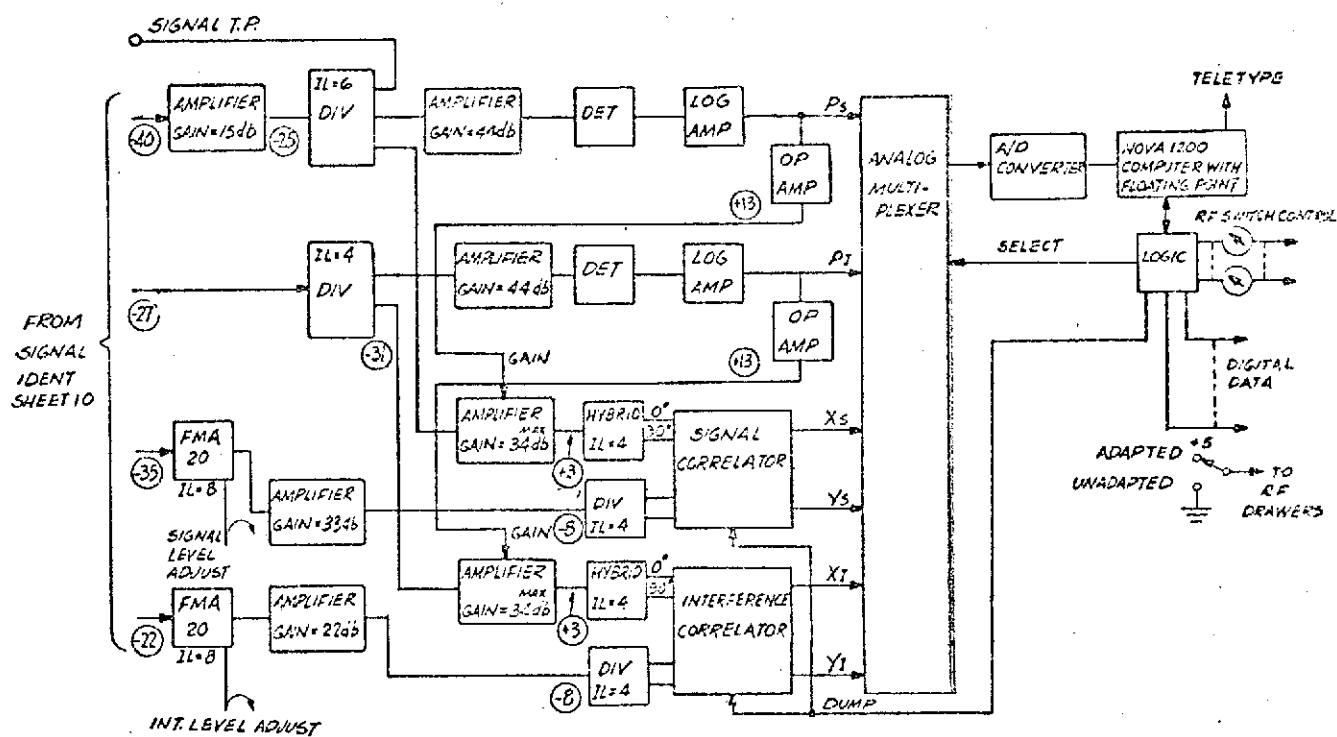


FIGURE 3-18B
DIGITAL PROCESSING ASSEMBLY CONTINUED

A second front panel control will enable the operator to clear the weights of the RF channels, but still maintain the computer-generated weights in a local memory. Application of this function quickly displays the difference between a final, adapted result and an unweighted beam. This difference should be evident by measurement with either a spectrum analyzer or the bit error rate tester.

The adaptive hardware should ideally operate over an unlimited dynamic range, since beam steering is useful regardless of signal power levels. However, several areas of hardware are subject to dynamic range limitations. One of these is the measurement ability of the computer with its A/D converter. An 8-bit converter was selected for the adaptive system upon the consideration that a higher number of bits would increase the conversion time and greatly increase the cost of the converter. The existing AGIPA system has been operating successfully with such an 8-bit converter.

The correlator units integration time will be under computer control which allows for rapid expansion or reduction in correlator bandwidth as a function of signal to interference ratio. A high-speed CMOS dump circuit has been added to the correlator units to reduce the computer waiting time.

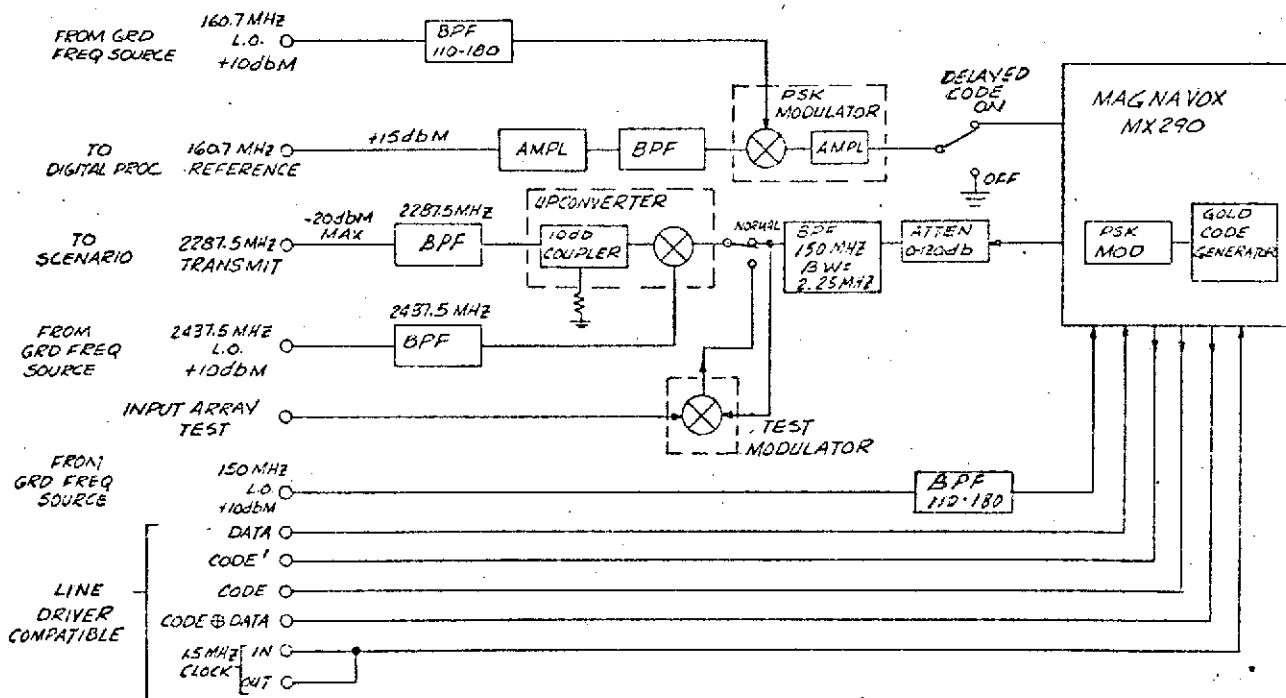
3.3.4 USER TRANSMITTER ASSEMBLY

INITIAL TESTING OF SYSTEM EMPLOYS SIMULATED USER SIGNAL. SUPPLYING BOTH THE DESIRED USER ENCODED SIGNAL AND A DELAYED REFERENCE, THE USER TRANSMITTER ASSEMBLY ALLOWS FOR CLOSED LOOP OPERATION WITHOUT ACTUAL USER.

The User Transmitter drawer, shown in Figure 3-19, is divided into four modules: (1) the Gold code Generator and Modulator, (2) the Upconverter, (3) the PSK Modulator, and (4) the Test modulator. The first of these generates a pseudo-random "Gold" code for spectrum spreading and modulo-2 adds the user message data. The resulting code is used to bi-phase modulate a 150 MHz carrier supplied by the system frequency source. The Upconverter mixes this signal with a 2437.5 MHz LO to produce the 2287.5 MHz user transmitter signal. The Gold code and data sum is also used in the third unit, where it is mixed with 160.7 MHz. This PSK signal is the reference signal for the digital processing assembly, where it is used to both despread the received 150 MHz user signal and convert it to 10.7 MHz. The fourth module provides AM modulation of the transmitted user signal. This function is employed only when antenna patterns of the adapted array are to be measured.

The Gold code generator employed in the user transmitter is identical to the generators found in the scenario interference sources. A complete description of these units may be found in Section 3.1. The clock for the user generator is the 1.5 MHz signal supplied by the system frequency source. The variable-rate (1, 10, 30, or 100 kbps) data available from the control section is modulo-2 added to the Gold code using an exclusive OR gate. The resulting code is sent to a PSK modulator which translates the signal to a 150 MHz bi-phase spectrum. A further upconversion to 2287.5 MHz completes the process. In a similar manner a delayed version of the code is employed to PSK modulate a 160.7 MHz reference signal. This signal is employed by the digital processing unit for despreading purposes.

The bi-phase modulated 150 MHz is passed through a variable attenuator and translated to 2287.5 MHz by means of a 2437.5 MHz signal from the satellite assembly. The bandpass filter, which follows, is there to eliminate both LO leakage and spurious mixer products. The required level of -20 dBm is subsequently sent to the transmitter antenna.



173-2651

FIGURE 3-19
USER TRANSMITTER ASSEMBLY

The attenuator located at 150 MHz can attenuate the signal up to 132 dB in 1 dB steps.

In order to prevent the 2287.5 MHz from feeding through the LO line back to the satellite, a narrow bandpass filter at 2437.5 MHz is used. This filter should provide 90 dB rejection at 2287.5 MHz.

This test modulator consists simply of a double-balanced mixer with DC coupled IF. A low frequency can thus be injected to AM-modulate the transmit signal before upconversion. This modulator allows the transmit signal to be amplitude modulated at rates around 1 kbps which is generally employed for antenna patterns.

3.3.5 GROUND STATION FREQUENCY SOURCE

UNIT SUPPLIES ALL OF THE FREQUENCIES REQUIRED BY THE TDRS GROUND STATION. ACCEPTING THREE REFERENCE SIGNALS FROM THE STATION REFERENCE THE GROUND STATION FREQUENCY SOURCE GENERATES REQUIRED SIGNALS FROM LOW FREQUENCY SYSTEM CLOCKS TO A 600 MHz PILOT FOR THE SATELLITE PHASE LOCKED FREQUENCY SOURCE.

By referring to Figure 3-20, it may be seen that the ground station frequency source accepts three input signals from the station reference. These signals are 5.0 MHz, 1 MHz, and 0.1 MHz. The 1 MHz and 0.1 MHz signals are used to generate the low frequency CW and clocks required. The manner in which this is accomplished is quite straightforward. The first step is a multiplication of the incoming signal to a frequency that is a higher harmonic of the frequency desired. A subsequent conversion to TTL logic allows for the eventual digital division to the required frequency.

The 5.0 MHz reference signal is multiplied by two to yield 10.0 MHz and then employed as a reference signal in a 50 MHz phase locked loop. The 50 MHz phase locked loop is a means of getting a times five multiplication of the reference 10.0 MHz and also achieve an increase in the signal to spurious level. The 50 MHz signal output from the loop, which is at a level of approximately 100 MW, is fed into a step recovery diode spectrum generator. The resultant of this process is to obtain a comb-like generation of signals at 50 MHz intervals. The appropriate signals are filtered and employed to either produce more frequencies or are sent to their appropriate assembly.

The super and subgroup frequency modules are described in section 3.2.4 and their description will not be repeated here.

Included within the ground station frequency source is the ground terminal forward link multiplexer shown in Figure 3-21. This unit accepts the 600 MHz pilot signal from the ground station frequency and combines it with the forward link data at 606.40625. The combined signal is then forwarded either directly to the satellite or in normal operation to the K_u -band uplink.

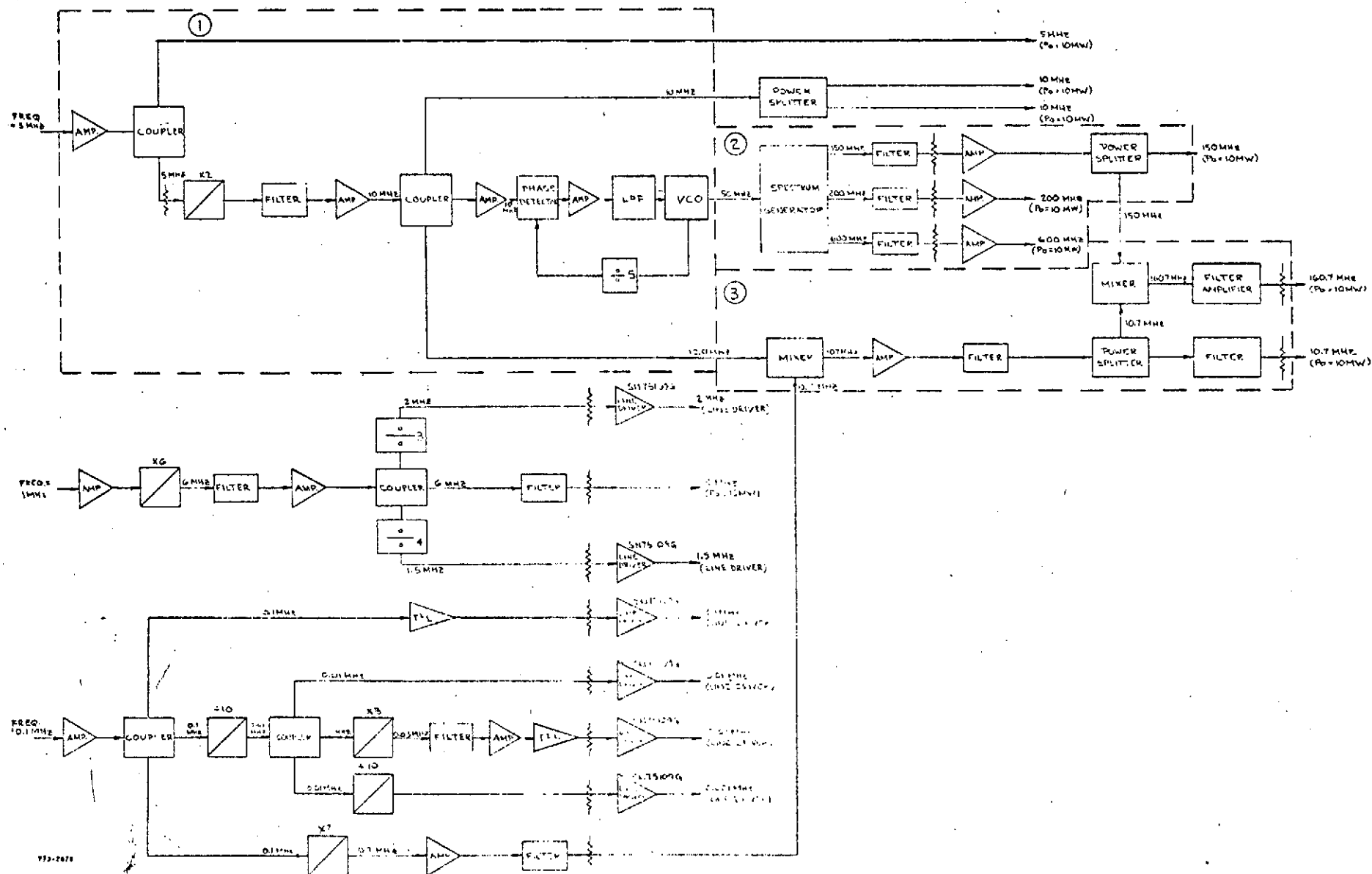


FIGURE 3-20
GROUND STATION FREQUENCY SOURCE

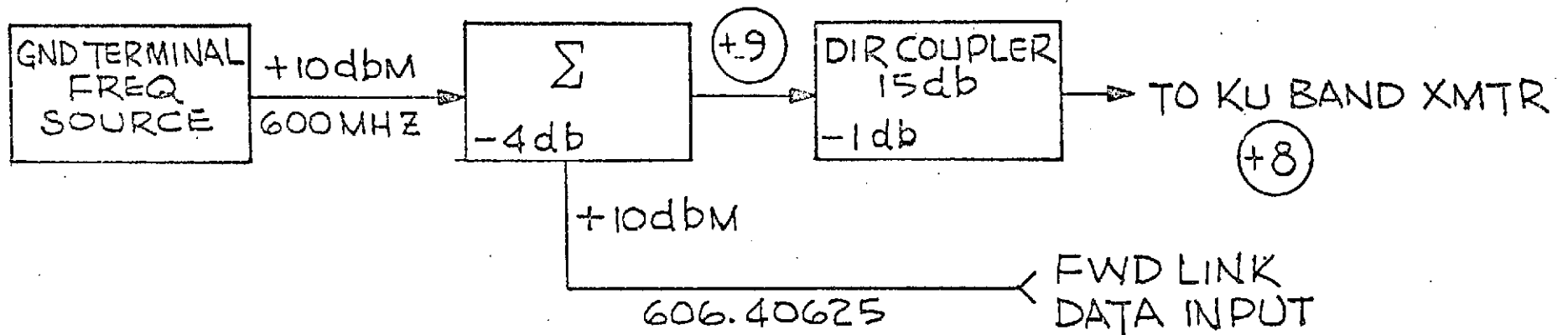


FIGURE 3-21
FORWARD LINK MULTIPLEXER

3.3.6 CONTROL-POWER SUPPLY

MONITORING, TESTING, DATA DETECTION AND DC POWER ARE FUNCTIONS OF THIS ASSEMBLY. BY PROVIDING MULTIPLE FRONT PANEL CONTROLS SYSTEM PERFORMANCE AND CONTROL AT VARIOUS STAGES FROM USER TRANSMITTER MODE TO INTERFERENCE LEVELS CAN BE BOTH MAINTAINED AND DIRECTED BY THE CONTROL UNIT.

The control section provides monitoring and testing functions for the ground equipment. It also provides for control of the scenario section. Data for the desired user is generated and tested in this unit. The functions of this section are:

- 1) Provide readouts of ground station power supply voltages.
- 2) Provide readout of Real and Imaginary components for each RF channel.
- 3) Generate a timing clock for each of the data rates required by the desired user.
- 4) Generate data for the desired user.
- 5) Verify the combination of code and data at the user transmitter by recovering the data and counting errors.
- 6) Detect the data from the array's resultant beam and measuring error rate.
- 7) On/Off and amplitude control functions for the ten interfering users.
- 8) Provide all necessary DC power.

1. The digital panel meter from the existing control unit will be used to monitor power supply voltages by inserting the meter plug into the "power supply test" jack. The display, accurate to ± 10 mv, exceeds the requirements of the RF and digital hardware.

2. The digital panel meter will provide readout of imaginary and real weighting voltages. Group selector and channel selector knobs will choose the desired channel, and a phase/attenuation switch will pick the voltage to be connected to the test jack. The meter accuracy

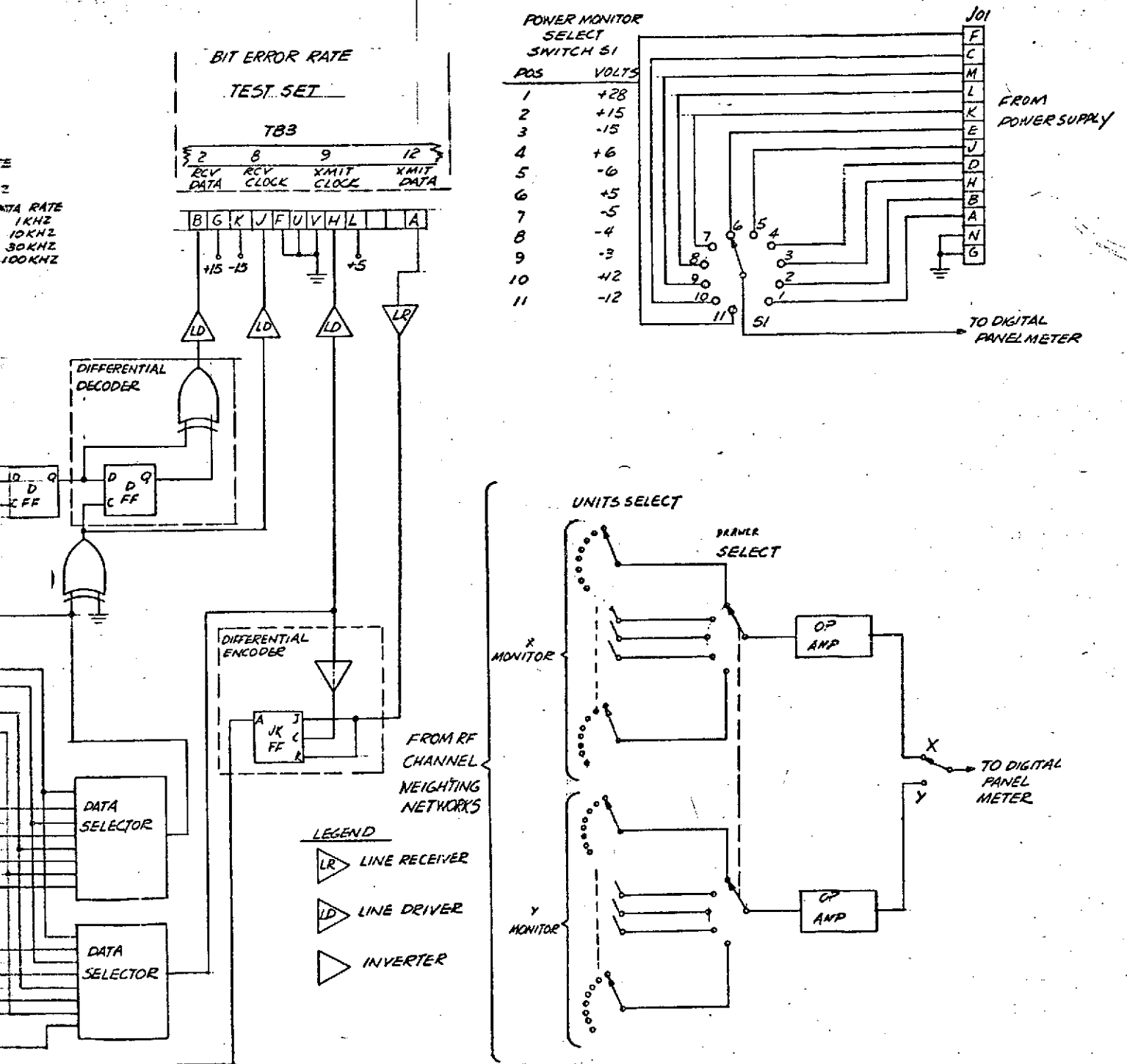
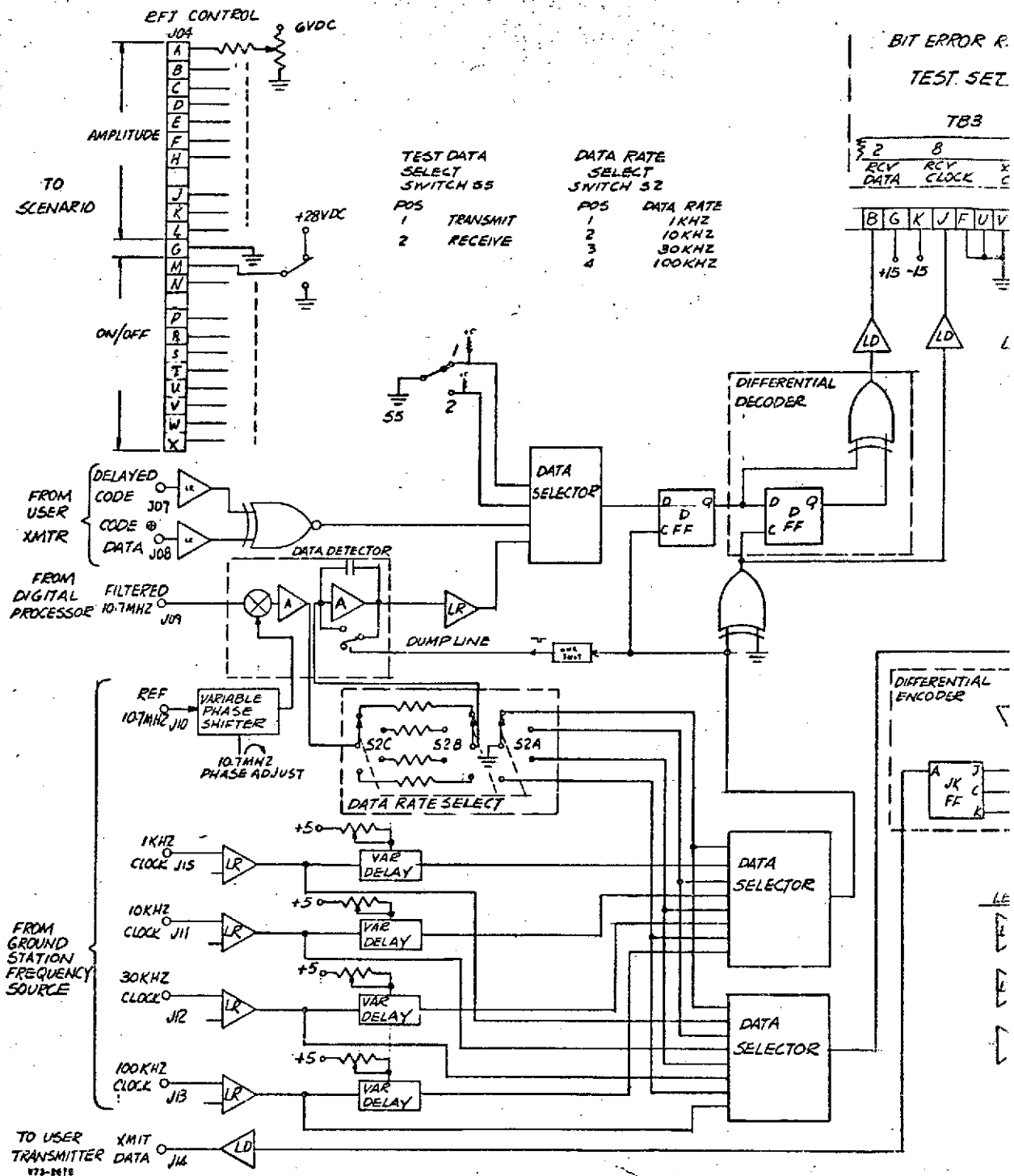


FIGURE 3-22
CONTROL UNIT ASSEMBLY



of ± 10 mv exceeds the 80 mv divisions between steps of the digitally-controlled weighting networks. Operational amplifiers are included so that the measurement does not load the channel weighting networks.

3. Four frequencies corresponding to the available data rates are provided by the frequency source. A front-panel control selects one of these rates (1, 10, 30 or 100 kbps). A line receiver squares off the clock signal waveform. This clock is connected directly to the bit error rate tester (BERT) to synchronize the user data. The clock is also delayed for synchronizing the received data. A separate variable delay is provided for each rate. The timing circuit for each monostable should only need one calibration.

4. The bit error rate tester (BERT) generates a pseudo-random data sequence for the desired user. Sequence lengths of 63, 127, 511, 1023, 2047 and 32767 bits are available. Other outputs available are "Mark" (all 1's), "Space" (all 0's) and "1:1" (square wave). Previous experience with the AGIPA system has revealed that occasional phase reversals occur in the received data, causing unnecessary errors. To eliminate these errors, differential encoding and decoding of data is employed. The encoding is accomplished with a J-K flip-flop. The coding is accomplished with a D flip-flop (one bit delay) and an exclusive OR gate. With differential encoding, the "Mark" is transmitted as a square wave, the "Space" as either a constant one or zero, and the "1:1" becomes a half-frequency square wave. These waveforms are also recovered by differential decoding.

5. Delayed code and code \oplus data are hardwired from the user transmitter. The control unit performs modulo-2 addition to recover the transmitted data. This data is synchronized with the delayed clock and sent to BERT. This function provides verification of the transmitted data.

6. The filtered 10.7 MHz from the summed channel of the digital processing unit contains the desired data. A 10.7 MHz reference frequency is adjusted with a phase shifter for phase coherency during calibration. The biphase PSK data may then be recovered by synchronous detection.

A Texas Instruments Type SN76514 integrated circuit balanced mixer is used to find the product of the 10.7 MHz signal and the 10.7 MHz reference. This mixer is an active device with gain. The signal input, however, must be limited, so that the threshold type detector that follows will operate over a large range of signal power.

The mixer is followed by two LM318 wideband operational amplifiers. The second of these is connected in the integrating mode to detect the DC-portion of the mixer output. These operational amplifiers were chosen for their wide bandwidth (15 MHz small-signal bandwidth) so that all system data rates will be handled. Dumping of the integrator is accomplished with a D-MOS transistor. This device has high speed and low on-resistance. A line receiver acts as a threshold device, or Schmitt trigger, to make the decisions on data.

The system data bandwidth requirements are dependent upon the spread-spectrum chip rate and the information bearing symbol rate. The channel bandpass is fixed by the limited spectrum occupancy allowed for the system. The chip rate of the spread spectrum coding is equal to 1.5 Mbps. The channel bandwidth is 2.25 MHz. This should provide negligible distortion of the spread-spectrum code. The processing gain for a one kilobit data signal and the above spread spectrum coding is 31.76 dB. Processing gain for 10 Kbps, 30 Kbps and 100 Kbps data rates are respectively 21.76 dB, 17 dB and 11.76 dB. To limit out of band interference in the AGIPA system the bandpass filters actually selected for the system closely approximate ideal bandpass characteristics.

The detector bandwidth has been selected to optimize the signal-to-noise ratio at the decision circuitry so as to minimize the probability of error. The optimum detector is a matched filter. For a PSK signal this is a multiplier whose local oscillator carrier is coherent with the received signal and whose output is processed by an integrate and dump circuit. At the termination of each pulse duration a decision is made as to the identity of the received signal based on the output of the integrator. In theory any predetection filtering has some effect upon the operation of the matched filter. However, with the predetection filter processing a 2.5 MHz bandpass and the data at rates of one to 100 kilobits, the effects are negligible.*

*Filter Distortion and Intersymbol Interference Effects on PSK Signals
J. Jay Jones, IEEE Trans. Comm. Tech., April 1971, pp. 120-132

The error probability for the AGIPA system should closely approximate the ideal probability of error curve. Since coherency is maintained in the system by hardwire connection, all reference signals are noise-free, and since matched filter detection will be employed, it is expected that the probability of error (P_e) will follow the ideal probability of error function for PSK signals. The error probability for the PSK is expressed as:

$$P_e = 1/2 \left[1 - \operatorname{erf} \left(\sqrt{E/N_0} \right) \right]^{1/2}$$

where E/N_0 represents the ratio of the energy per bit to the noise spectral density. ** How close the actual circuitry of the system can match theory will be directly measurable by the control assembly and will be in itself a measure of the quality of the system's performance.

7. The ten interfering users are described in detail in another section. The on/off and amplitude controls for these users are included in this unit in order to be near the desired user transmitter control. The on/off switches control the +28 volt power supply for each of the ten oscillators. Potentiometers are used to set the amplitude control voltages from 0 to +6 volts.

8. Modular power supplies will be employed by the system. Each unit will be over voltage protected and will possess a capacity rating in excess of its known power requirements to allow for possible expansion. Regulation of each supply shall be 0.1% or better. A detailed listing of supply specifications appears in appendix .

**Ibid

APPENDIX I

MAJOR SYSTEMS COMPONENT SPECIFICATIONS

This appendix contains a listing of the electrical specifications of units employed in the TDRS Simulation System. The formal specifications, generated by AIL, for both the S-band Downconverter and the system filter requirements are included in this appendix. The remainder of the specifications are listed for reference and are the vendor specifications for commercially available components.

BANDPASS FILTER SPECIFICATION NO. 1001

Center Frequency:	150 MHz
3 dB bandwidth:	3.75 MHz minimum
30 dB bandwidth:	6 MHz maximum
60 dB bandwidth:	12 MHz maximum
Ultimate attenuation:	Greater than 60 dB
Input/output impedance:	50 ohms
Phase Linearity 3 MHz bandwidth:	$\emptyset \quad \underline{+10}$
Phase tracking 3 MHz bandwidth:	$\underline{+5}^{\circ}$
Ripple maximum:	0.1 dB
VSWR within 3 MHz bandwidth:	1.5:1

BANDPASS FILTER SPECIFICATION NO. 1002

Center frequency:	110 MHz
0.5 dB bandwidth:	3 dB bandwidth of specification No. -01
60 dB bandwidth:	70 MHz
Ultimate attenuation (DC-500 MHz):	60 dB
Input/output impedance:	50 ohms
Phase linearity within 0.5 dB bandwidth:	$\underline{+3}^{\circ}$
Ripple maximum:	0.1 dB

In addition to the above, pairs of filters must phase track or provide equal time delays over the 3 dB bandwidth to within $+5^{\circ}$ tolerance. The pairs of filters which must exhibit this characteristic are:

60 MHz-110 MHz; 74 MHz-104 MHz;
80 MHz- 98 MHz; 86 MHz-92 MHz

With the exceptions noted, the following filters all are as specified above:

A.	Center Frequency	104 MHz
	Quantity	8
B.	Center Frequency	98 MHz
	Quantity	8
C.	Center Frequency	92 MHz
	Quantity	8
D.	Center Frequency	86 MHz
	Quantity	8
E.	Center Frequency	80 MHz
	Quantity	8
F.	Center Frequency	74 MHz
	Quantity	8
G.	Center Frequency	68 MHz
	Quantity	8

BANDPASS FILTER SPECIFICATION NO. 1003

Center Frequency:	89 MHz
0.5 dB bandwidth	48 MHz
Rejection at 218-260 MHz:	60 dB
Phase linearity:	$\pm 5^\circ$
Input/output impedance:	50 ohms
VSWR with 0.5 dB bandwidth:	1.5:1
Bandwidth tolerance:	$-0 + 1\%$
Ripple maximum:	0.1 dB
Phase track:	$\pm 5^\circ$

BANDPASS FILTER SPECIFICATION NO. 1004

Center Frequency:	295 MHz
0.5 dB bandwidth (min.):	48 MHz
Rejection at 384 MHz:	60 dB
Rejection at DC-150 MHz:	60 dB
Maximum insertion loss:	3 dB
Phase linearity:	$\pm 5^\circ$
Ripple maximum:	0.1 dB
Bandwidth tolerance:	$-0, +1\%$

In addition to the above pairs of filters must track or provide equal time delays over the 3 dB bandwidth to within $\pm 5^\circ$ tolerance. The pairs of filters which must exhibit this characteristic are: 295-439 MHz; 343-391 MHz.

BANDPASS FILTER SPECIFICATION NO. 1005

Same as specification No. -04 with the following line exceptions:

Center frequency:	343 MHz
Rejection at 432 MHz	60 dB

BANDPASS FILTER SPECIFICATION NO. 1006

Same as specification No. -04 with the following line exceptions:

Center frequency:	391 MHz
Rejection at 480 MHz:	60 dB

BANDPASS FILTER SPECIFICATION NO. 1007

Same as specification No. -04 with the following line exceptions:

Center frequency:	439 MHz
Rejection at 528 MHz	60 dB

BANDPASS FILTER SPECIFICATION NO. 1008

Center frequency:	367 MHz
0.5 bandwidth:	200 MHz
Rejection 734-1500 MHz	50 dB
Rejection DC-180 MHz	50 dB
Maximum insertion loss:	3.0 dB
Phase linearity:	$\pm 5^\circ$
Ripple maximum:	0.1 dB
Bandwidth tolerances:	0, $\pm 2\%$

S-BAND DOWNCONVERTER SPECIFICATION NO. 4212

1. General

The S-band Downconverter will be used to expand the capabilities of the existing AGIPA hardware by increasing the number of channels and duplicating the characteristics of the existing RF portion of the satellite equipment.

2. RF Input Frequency

The RF Input Frequency shall be within a minimum downconverter RF input passband of 2287.5 MHz.

3. Output IF Frequency

The output IF frequency shall be centered at 150 MHz for operation at the nominal input frequency of 2287.5 MHz and an LO frequency of 2437.5 MHz.

4. Input Power

The downconverter shall meet the requirements of this specification for input power levels of sensitivity to -65 dBm.

5. Local Oscillator Power

The downconverter shall meet the requirements of this specification for LO input power levels of +7 dBm \pm 1 dB

6. RF to IF Gain

The RF to IF gain shall be a minimum of 33 dB and shall be constant to \pm .5 dB over the temperature range of 0° to 40°C.

7. Gain and Phase Tracking

The design of the S-band downconverter shall be such that over the IF frequency band of 150 ± 2.0 MHz and at any given RF input power within the full dynamic range, all units shall track to within ± 0.2 dB of a linear gain response and within $\pm 1.0^\circ$ of a linear phase response.

8. Impedance

The impedance of all ports shall be a nominal 50 ohms with a VSWR of 1.3:1 or less.

9. Load Impedance

The unit will operate into a nominal load impedance of 50 ohms and shall meet the requirements of this specification for VSWR variations up to 2:1. All units shall be unconditionally stable when operating into any VSWR at any port.

10. IF Bandwidth

The S-band downconverter shall have a minimum IF bandwidth of 20 MHz centered at the IF frequency specified in paragraph 3.

11. Noise Figure

The S-band downconverter shall have a SSB input noise figure of 12 dB or less at the RF input frequency specified in paragraph 2.

12. EMC

The S-band downconverter shall be contained in a shielded package such that radiation from the units shall be down -100 dB at a distance of 0.5 meter from the unit. Any RF or IF signals appearing on the power lines shall be no greater than -100 dBm.

FMA-131 THIN FILM WIDE BAND HYBRID AMPLIFIER

SPECIFICATIONS

Frequency Range	5 to 550 MHz
Gain	21 dB
Gain Flatness	+0.5 dB
Noise Figure	5 dB
VSWR	1.25:1
Power Output, 1 dB Compression	+10 dBm
Power Supply	+12 VDC, 54 ma

FMA-135 THIN FILM WIDE BAND HYBRID AMPLIFIER

SPECIFICATIONS

Frequency Range	5 to 550 MHz
Gain	32 dB
Gain Flatness	+0.75 dB
Noise Figure	4 dB
VSWR	1.25:1
Power Output, 1 dB Compression	+10 dBm
Power Supply	+12 VDC, 64 ma

FMA-20 THIN FILM WIDE BAND HYBRID ATTENUATOR

SPECIFICATIONS

Frequency Range	5 to 1,000 MHz
Attenuation Range	20 dB
VSWR	1.3:1
RF Input Power	+6 dBm
Power Supply	+12 VDC, 7 ma

MODEL PSC-2-1 TWO WAY POWER SPLITTER SPECIFICATIONS

Frequency Range (MHz)	.1-400 MHz	
Nominal Phase Difference Between Output Ports	0°	
Impedance, All Ports	50 ohms	
Isolation Between Output 1 and 2, dB	Typical	Minimum
2 - 40 MHz	40	30
.4 - 400 MHz	25	20
.1 - .4 MHz	20	15
Insertion Loss, dB (above 3 dB split)	Typical	Minimum
.1 - 100 MHz	.2	.5
100 - 200 MHz	.4	.75
200 - 400 MHz	.6	1.0
Phase Unbalance, degrees	Typical	Minimum
0.1 - 100 MHz	.5	2
100 - 200 MHz	1	3
200 - 400 MHz	2	4
Amplitude Unbalance, dB	Typical	Minimum
.1 - 100 MHz	.05	.15
100 - 200 MHz	.05	.2
200 - 400 MHz	.1	.3
VSWR	1.2 typical	
Matched Power Rating	1 watt maximum	
Internal Load Dissipation	1/8 watt	

MODEL MSC-2-1 TWO WAY POWER SPLITTER SPECIFICATIONS

Frequency Range (MHz)	0.1 - 450 MHz	
Nominal Phase Difference Between Output Ports	0°	
Impedance, All Ports	50 ohms	
Isolation, dB, between Output 1 and 2	Typical	Minimum
- 250 MHz	35	30
0.4 - 450 MHz	30	20
0.1 - 0.4 MHz	20	15
Insertion Loss dB (above 3 dB split)	Typical	Minimum
20 - 100 MHz	.3	.5
100 - 250 MHz	.4	.75
200 - 450 MHz	.6	1.0
Phase Unbalance, degrees	Typical	Minimum
0.1-100 MHz	.5	2
100 - 200 MHz	1	3
200 - 400 MHz	2	4
Amplitude Unbalance, dB	Typical	Minimum
.1 - 100 MHz	.05	.15
100 - 200 MHz	.05	.2
200 - 450 MHz	1	.3
VSWR	1.2 typical	
Matched Power Rating	1 watt maximum	
Internal Load Dissipation	1/8 watt	

SRA-1W DOUBLE BALANCED MIXER

SPECIFICATIONS:

Frequency range, MHz	LO	1-750	
	RF	1-750	
	IF	DC-750	
		Typical	Maximum
Conversion Loss, dB one octave from band edge		5.5	7.5
Total range		6.5	8.5
Signal, 1 dB Compression level		+1 dBm	
Isolation, dB		Typical	Minimum
Lower band edge to one decade higher	LO-RF	50	45
	LO-IF	45	30
Mid range	LO-RF	45	30
	LO-IF	40	25
Upper band edge to one octave lower	LO-RF	35	25
	LO-IF	30	20
Impedance, all ports		50 ohms	
Phase Detection			
DC offset		1 mV typical	
DC polarity		Negative	
Electronic Attenuation			
Minimum Attenuation (20mA)		3.5 dB	

MO-108 DOUBLE BALANCED MIXER

SPECIFICATIONS:

Frequency Range:

LO (L) Port	5-500 MHz
RF (R) Port	5-500 MHz
IF (X) Port	DC-500 MHz

Isolation (db min.):

	L-R	L-X	R-X
5-150 MHz	40	35	25
150-500 MHz	34	25	20

Impedance	50 ohms
-----------	---------

Conversion Loss:

5-150 MHz	7.0 db Max
150-500 MHz	9.0 db Max.

APPENDIX II

CIRCUIT PHASE ERROR EFFECTS

In order to specify the phase accuracy desired for the electronic circuits, the effects of adding N signals, each with a random phase term, is investigated. The sum of these signals (P_S) is equal to:

$$P_S = \sum_i^N A \cos (\omega_o t + \psi_i)$$

where ψ_i is assumed to be uniformly distributed across the array electronic elements between $\pm \epsilon$. Using a trigonometric identity, the signal term, P_S , can be expanded as

$$P_S = \sum_i^N A (\cos \omega_o t \cos \psi_i - \sin \omega_o t \sin \psi_i)$$

Expanding the $\cos \psi_i$ and $\sin \psi_i$, into a trigonometric series and using only the first two terms, results in

$$\begin{aligned} \frac{P_S}{A} &= N \cos \omega_o t - \sum_i^N \psi_i \sin \omega_o t \\ &\quad - \sum_i^N \frac{\psi_i^2}{2} \cos \omega_o t + \frac{\psi_i^3}{6} \sin \omega_o t \end{aligned}$$

The term $N \cos \omega_o t$ represents the desired signal term and the remaining terms are distortion terms generated by phase errors.

The objective is to determine the value of the signal term relative to the phase distortion term, such that limits can be placed on the value of ϵ , which will define the permissible phase tolerance on the individual electronic circuits.

Assuming that the phase error, ϵ , is less than a radian, the high order terms are neglected and the remaining distortion term is

$$\frac{P_n}{A} = \sum_i^N \psi_i \sin \omega_o t$$

where ψ_i is uniform $(-\epsilon, \epsilon)$ and has a density function

$$p(\psi_i) = \frac{1}{2\epsilon}$$

To find the average power of P_n , the variance of the sum

$$V = \sum_{i=1}^N \psi_i$$

must be evaluated. The variance of the sum of a series of independent random variables

$$V = \psi_1 + \psi_2 + \dots + \psi_n$$

is equal to the sum of the variances for a large number of elements. Therefore,

$$\sigma_V^2 = \sigma_1^2 + \sigma_2^2 + \dots + \sigma_N^2$$

The variance of ψ_i can be found as follows

$$\sigma_1^2 = E[\psi_i^2] = \int_{-\epsilon}^{\epsilon} \psi_i^2 p(\psi_i) d\psi_i = \frac{2}{3}$$

$$\text{therefore } \sigma_V^2 = \frac{N\epsilon^2}{3}$$

Thus, the average power due to the phase distortion is

$$\overline{P_n} = V^2 \sin^2 \omega t = \frac{1}{2} \frac{N\epsilon^2}{3}$$

For the signal term

$$P_S = N \cos^2 \omega_0 t$$

The average is

$$P_S^2 = \frac{N^2}{2}$$

Therefore, the signal to phase distortion is

$$\rho = \frac{\frac{N^2}{2}}{\frac{N\epsilon^2}{6}} = \frac{3N}{\epsilon^2}$$

APPENDIX III

SPURIOUS ANALYSIS

The presence of many signals at the mixers of the simulation system can cause many unwanted spurious responses at the desired IF frequency. A computer analysis has been performed which accounts for every input signal at each mixer and generates the order of all resulting spurious responses within the IF bandwidth. This information along with a knowledge of the mixer characteristics allows the relative levels of the spurious responses to be predicted. The levels determine the amount of filtering which will be required.

Figure III-1 is a block diagram of the LO distribution. On many of these outputs adjacent LO frequencies will appear about 60 dB below the desired LO frequency. It is necessary to include these adjacent LO frequencies in the computer program as RF inputs. The results of the computer analysis shown in Table III-1 show that for the cases of RF interaction with the LO all inband spurs will be at least 88 dB below the desired IF output and all harmonics will be at least 74 dB below the desired IF output. Therefore, additional filtering will not be required to reduce spurs resulting from RF interaction with the LO. The spurious responses resulting from LO interaction with adjacent LO frequencies will result in spurious responses at the IF frequency and therefore, additional filtering will be required on the LO lines.

Tables III-2 through III-4 list all of the cases which the computer program analyzed. Table III-2 lists all of the cases where there was no LO interaction with adjacent LO frequencies. Tables III-3 and III-4 list all of the LO interaction cases. The first column is the number assigned to each LO. Column 2 is the desired LO frequency at a mixer. Column 4 lists all of the possible inputs which include the desired RF input and the other LO frequencies listed by assigned number. The last column is the IF frequency and the bandwidth over which the spurs will be listed.

The result of this analysis is that filters must be included on all LO lines in the MUX and DEMUX groups to attenuate the adjacent LO frequencies.

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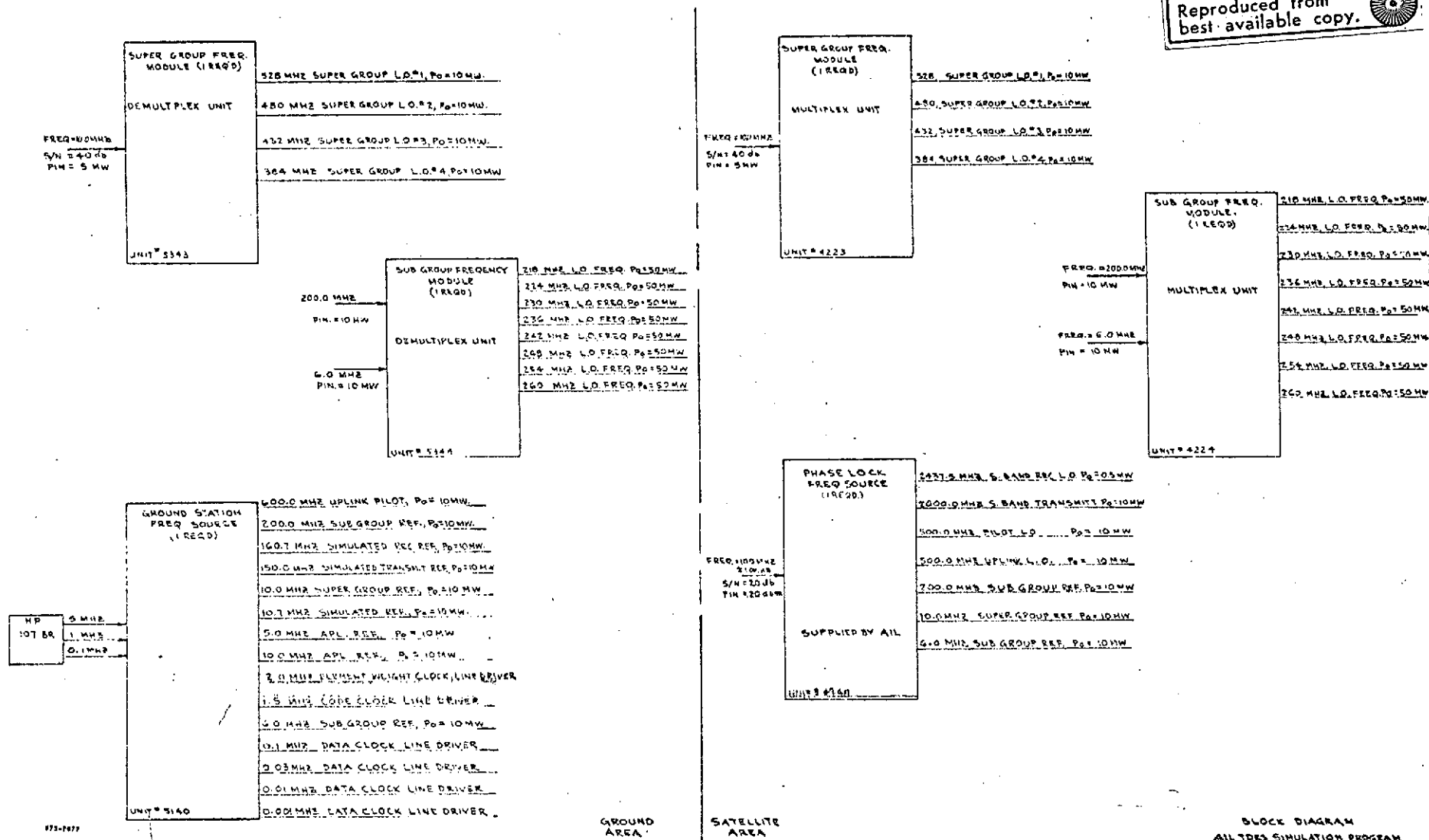


FIGURE III-1
TDRS L.O. DISTRIBUTION

TABLE III-1

COMPUTER SPUR ANALYSIS RESULTS

RF INTERACTION

- ALL 3 ORDER AND ABOVE INBAND SPURS ARE MORE THAN 88 dB
- ALL HARMONICS ARE AT LEAST 74 dB BELOW THE IF LEVEL

LO INTERACTION

- GROUND DEMUX SUPERGROUP
1 X 1 LO PRODUCTS FALL INBAND
ISOLATION NECESSARY REQUIRES 80 dB REJECTION OF OTHER LO FREQUENCIES
- SATELLITE MUX SUPERGROUP
DIRECT LEAKAGE
ISOLATION NECESSARY REQUIRES 80 dB REJECTION OF OTHER LO FREQUENCIES

TABLE III-2

COMPUTER SPUR ANALYSIS

SATELLITE ELEMENT	LO	INPUT	IF
IN	2437.5	2250 ± 100	150 ± 3
MUX	SEE CHART 2		
IMAGER	734	367 ± 100	367 ± 100
FWD LINK TRANSMIT	2000	106 ± 3	2106 ± 25
FWD LINK DATA	1 500	606 ± 3	106 ± 3
	2 500	$597.5 \pm .01$	$102.5 \pm .01$
	3 500	606 ± 3	$102.5 \pm .01$
	4 500	$597.5 \pm .01$	106 ± 3
GROUND	SEE CHART 3		
DEMUX	160.7	150 ± 1.5	10.7 ± 3
PN DETECTOR			

TABLE III-3
GROUND TERMINAL SPUR ANALYSIS

	LO	INPUTS	IF
DEMUX SUPER GROUP	1 384	295 \pm 25, LO (2, 3, 4)	89 \pm 50
	2 432	343 \pm 25, LO(1, 3, 4)	89 \pm 50
	3 480	391 \pm 25, LO (1, 2, 4)	89 \pm 50
	4 528	439 \pm 25, LO (1, 2, 3)	89 \pm 50
DEMUX SUB GROUP	1 218	68 \pm 1.5, LO (2, 3, 4, 5, 6, 7, 8)	150 \pm 3
	2 224	74 \pm 1.5, LO(1, 3, 4, 5, 6, 7, 8)	150 \pm 3
	3 230	80 \pm 1.5, LO (1, 2, 4, 5, 6, 7, 8)	150 \pm 3
	4 236	86 \pm 1.5, LO (1, 2, 3, 5, 6, 7, 8)	150 \pm 3
	5 242	92 \pm 1.5, LO (1, 2, 3, 4, 6, 7, 8)	150 \pm 3
	6 248	98 \pm 1.5, LO (1, 2, 3, 4, 5, 7, 8)	150 \pm 3
	7 254	104 \pm 1.5, LO (1, 2, 3, 4, 5, 6, 8)	150 \pm 3
	8 260	110 \pm 1.5, LO (1, 2, 3, 4, 5, 6, 7)	150 \pm 3

TABLE III-4
SATELLITE SPUR ANALYSIS

	LO	INPUTS	IF	
MUX SUB GROUP	1	218	150 \pm 3, LO (2, 3, 4, 5, 6, 7, 8)	68 \pm 3
	2	224	150 \pm 3, LO (1, 3, 4, 5, 6, 7, 8)	74 \pm 3
	3	230	150 \pm 3, LO (1, 2, 4, 5, 6, 7, 8)	80 \pm 3
	4	236	150 \pm 3, LO (1, 2, 3, 5, 6, 7, 8)	86 \pm 3
	5	242	150 \pm 3, LO (1, 2, 3, 4, 6, 7, 8)	92 \pm 3
	6	248	150 \pm 3, LO (1, 2, 3, 4, 5, 7, 8)	98 \pm 3
	7	254	150 \pm 3, LO (1, 2, 3, 4, 5, 6, 8)	104 \pm 3
	8	260	150 \pm 3, LO (1, 2, 3, 4, 5, 6, 7)	110 \pm 3
MUX SUPER GROUP	1	384	89 \pm 25, LO (2, 3, 4)	295 \pm 50
	2	432	89 \pm 25, LO (1, 3, 4)	343 \pm 50
	3	480	89 \pm 25, LO (1, 2, 4)	391 \pm 50
	4	528	89 \pm 25, LO (1, 2, 3)	439 \pm 50

APPENDIX IV

INTERFACE SPECIFICATIONS

This section defines the interface requirements between the equipment which is being supplied by AIL and that portion of the system which APL is integrating.

A-1 Ground Equipment

1. Return Link FDM input - Thirty channel multiplied input from K_u -band Receiver
 - Frequency: 606.40625 MHz
 - Power Level: +10 dBm
 - Impedance: 50 ohms
 - VSWR: 1.5 Input and Output Maximum
 - Spurious Inputs: 60 dB or greater below signal level
2. Forward Link RF Output - PN-PSK modulated command link signal.
 - Frequency: 2106.40625 MHz
 - Bandwidth: 3.75 MHz
 - Power Level: -23 dBm
 - Impedance: 50 ohms
 - VSWR: 1.5 max.
 - Spurious: 60 dB down

3. Forward Link FDM Output-FDM Input to K_u -band ground transmitter containing transponder command data and pilot tone for satellite phase lock loop reference.

Frequency:	Command	606.40625 MHz
	Pilot	600.0 MHz

Bandwidth: 10 MHz

Power Level: -5 dBm minimum

Impedance: 50 ohms

VSWR: 1.5 max.

Spurious: 60 dB down

4. Return Link Array Output

Frequency: 10.7 MHz

Bandwidth: 1 KHz, 10 KHz, 30 KHz, or 100 KHz

Power Level: Variable, -31 dBm max.

Impedance: 50 ohms

VSWR: 1.5 max.

Spurious: 60 dB down

5. Frequency Reference Outputs-Reference frequencies to which all K_u-band transceivers local oscillators are locked.

Reference A:

Frequency:	10 MHz
Impedance:	50 ohms
VSWR:	1.5 maximum
Spurious level:	60 dB down

Reference B:

Frequency:	5 MHz
Power level:	+10 dBm
Impedance:	50 ohms
VSWR:	1.5 maximum
Spurious level:	60 dB down

A-2 Satellite Equipment

1. Return Link FDM Output

Frequency: 271-463 MHz
Power level: -29 dBm peak
Impedance: 50 ohms
VSWR: 1.5:1 input/output maximum
Spurious level: 60 dB or greater below signal level

2. Forward Link FDM Input

Frequency: 606.40625 and 600.00 MHz
Power Level: -10 dBm minimum
Impedance: 50 ohms
VSWR: 1.5:1 input/output
Spurious Level: 60 dB or greater below lowest signal level

3. S-band Reference

Frequency: 2 GHz
Power level: +10 dBm
Impedance: 1.5:1 input/output
Spurious level: 60 dB below signal level

4. Low Frequency Reference A

Frequency: 10 MHz
Power Level: +10 dBm
Impedance: 50 ohms
VSWR: 1.5:1
Spurious Level: 60 dB below reference signal

5. Low Frequency Reference B

Frequency:	5 MHz
Power level:	+10 dBm
Impedance:	50 ohms
VSWR:	1.5:1 input/output
Spurious level:	60 dB below reference

A-3 Scenario Interface Requirements

1.0 Interference Data Modulation

- a. Connector - BNC
- b. Impedance - 93 ohms
- c. Balanced input compatible with SN75107AN line converter
- d. Differential input voltage
 - "0" state +25 mv
 - "1" state +25 mv
 - Maximum +3v
- e. The cable shield shall not be grounded
- f. Frequency Range 5 MHz

2.0 Forward Link RF Output

- a. Connector - Type N
- b. Impedance - 50 ohms
- c. VSWR - 1.5:1 at 2106 Mhz
- d. Antenna Peak Gain above isotropic radiation is 8 dBi
- e. Antenna is linearly polarized

3.0 Clock Input

- a. Connector - BNC
- b. Impedance - 93 ohms
- c. Balanced input compatible with SN75107AN line receiver
- d. Differential Input Voltage
 - "0" state +25 mv
 - "1" state +25 mv
 - Maximum +3v
- e. The cable shield shall not be grounded.
- f. Frequency range 7 MHz